

# Compal Confidential

## EH78F MB Schematic Document

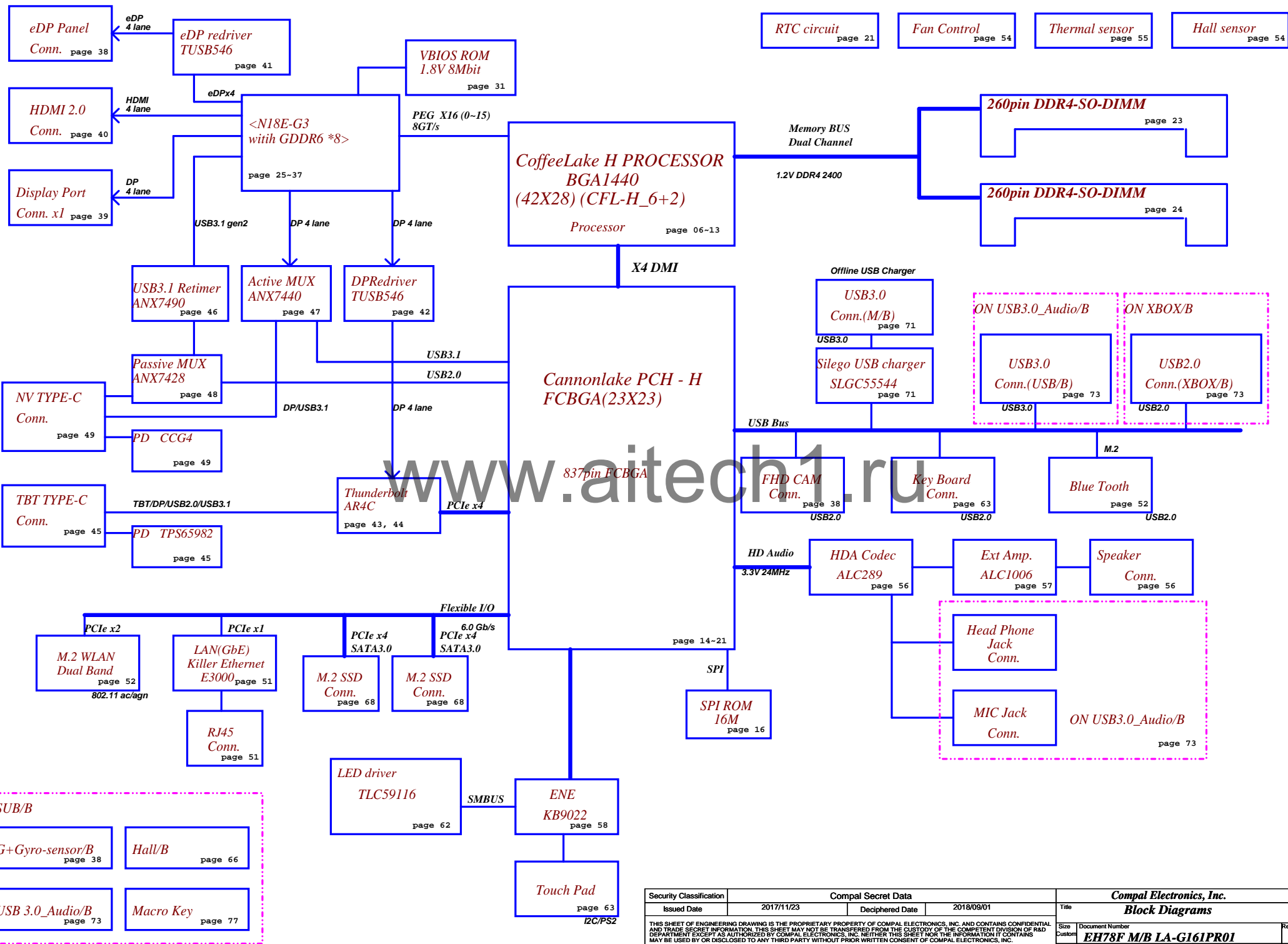
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LA-G161P

Rev:1C

2019.01.16

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Issued Date	2017/11/23	Deciphered Date	2018/09/01	Title	Cover Sheet
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Issued Date	2017/11/23	Deciphered Date	2018/09/01	Block Diagrams	
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Vcc	3.3V +/- 5%				
Ra	100K +/- 5%				
Board ID	Rb	V <sub>BI</sub> D min	V <sub>BI</sub> D typ	V <sub>BI</sub> D max	EC AD
0	0		0.000 V	0.300 V	0x00 - 0x13
1	12K +/- 1%	0.347 V	0.345 V	0.360 V	0x14 - 0x1E
2	15K +/- 1%	0.423 V	0.430 V	0.438 V	0x1F - 0x25
3	20K +/- 1%	0.541 V	0.550 V	0.559 V	0x26 - 0x30
4	27K +/- 1%	0.691 V	0.702 V	0.713 V	0x31 - 0x3A
5	33K +/- 1%	0.807 V	0.819 V	0.831 V	0x3B - 0x45
6	43K +/- 1%	0.978 V	0.992 V	1.006 V	0x46 - 0x54
7	56K +/- 1%	1.169 V	1.185 V	1.200 V	0x55 - 0x64
8	75K +/- 1%	1.398 V	1.414 V	1.430 V	0x65 - 0x76
9	100K +/- 1%	1.634 V	1.650 V	1.667 V	0x77 - 0x87
10	130K +/- 1%	1.849 V	1.865 V	1.881 V	0x88 - 0x96
11	160K +/- 1%	2.015 V	2.031 V	2.046 V	0x97 - 0xA4
12	200K +/- 1%	2.185 V	2.200 V	2.215 V	0xA5 - 0xAF
13	240K +/- 1%	2.316 V	2.329 V	2.343 V	0xB0 - 0xB7
14	270K +/- 1%	2.395 V	2.408 V	2.421 V	0xB8 - 0xBF
15	330K +/- 1%	2.521 V	2.533 V	2.544 V	0xC0 - 0xC9
16	430K +/- 1%	2.667 V	2.677 V	2.687 V	0xCA - 0xD4
17	560K +/- 1%	2.791 V	2.800 V	2.808 V	0xD5 - 0xDD
18	750K +/- 1%	2.905 V	2.912 V	2.919 V	0xDE - 0xFF
19	NC	3.000 V	3.000 V		0xF1 - 0xFF

BUS	Device	Address(7 bit)	Address(8bit)	
			Write	Read
I2C_0 (+3VS)	LIS2DH12TR (G-sensor)			
I2C_1 (+3VS)	TM-03461-001 (Touch Pad)			
PCH_SMBCLK (+3VALW)	DIMM1			
	DIMM2			
PCH_SML1CLK EC_SMB_CK2 (+3VALW)	N18E-G3 (VGA)	0x9E		
	TMS(NCT7718W )hot	0x98		
	TMS(W83L771AWG-2 )cool	0x9A		
	LIS2DH12TR(M/B)			
	LIS2DH12TR(SUB/B)			
EC_SMB_CK1 (+3VLP)	ISL88739 (Charger IC)	0x11		
	BATTERY PACK	0x16		
EC_SMB_CK3 (+3VALW)	PD(TPS65982)	0x70		
	LED driver	0xC0		
EC_SMB_CK4 (+3VALW)				

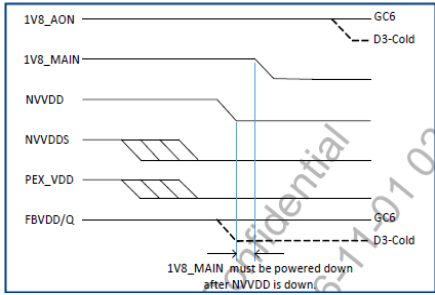
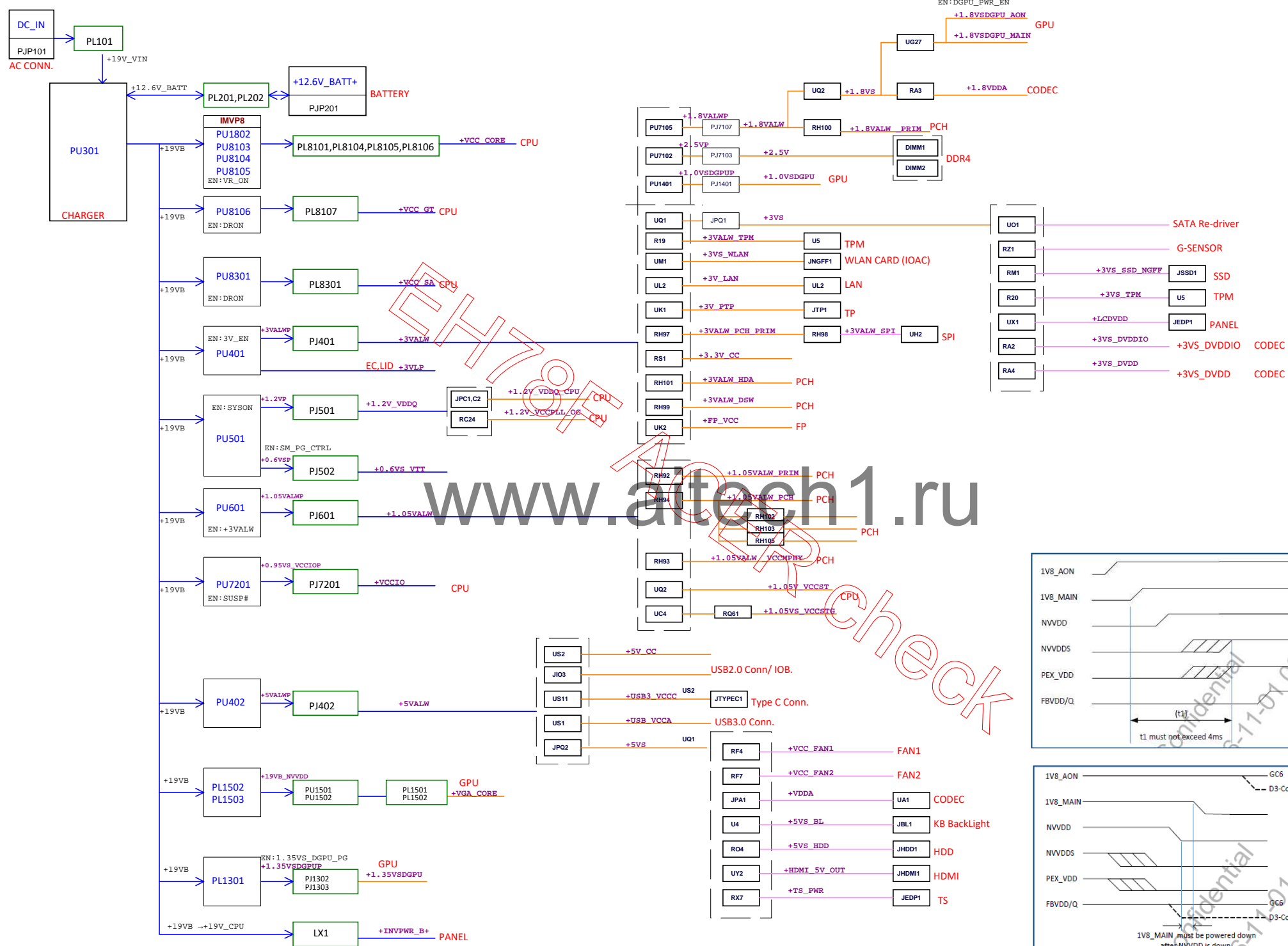
[illegible][illegible]

<i>STATE</i> \ <i>SIGNAL</i>	<i>SLP_S3#</i>	<i>SLP_S4#</i>	<i>SLP_S5#</i>	<i>+VALW</i>	<i>+V</i>	<i>+VS</i>	<i>Clock</i>
<i>S0 (Full ON)</i>	<i>HIGH</i>	<i>HIGH</i>	<i>HIGH</i>	<i>ON</i>	<i>ON</i>	<i>ON</i>	<i>ON</i>
<i>S3 (Suspend to RAM)</i>	<i>LOW</i>	<i>HIGH</i>	<i>HIGH</i>	<i>ON</i>	<i>ON</i>	<i>OFF</i>	<i>OFF</i>
<i>S4 (Suspend to Disk)</i>	<i>LOW</i>	<i>LOW</i>	<i>HIGH</i>	<i>ON</i>	<i>OFF</i>	<i>OFF</i>	<i>OFF</i>
<i>S5 (Soft OFF)</i>	<i>LOW</i>	<i>LOW</i>	<i>LOW</i>	<i>ON</i>	<i>OFF</i>	<i>OFF</i>	<i>OFF</i>

Power Plane	Description	S0	S3	S4	S5
+RTC_VCC	RTC Battery Power	ON	ON	ON	ON
+19V_VIN	Adapter power supply	N/A	N/A	N/A	N/A
+12.6V_BATT	Battery power supply	N/A	N/A	N/A	N/A
+19VB	AC or battery power rail for power circuit.	N/A	N/A	N/A	N/A
+3VLP	+19VB to +3VLP power rail for suspend power	ON	ON	ON	ON
+5VALW	+5V Always power rail	ON	ON	ON	ON
+3VALW	System +3VALW always on power rail	ON	ON	ON	ON*
+3VALW_DSW	+3VALW power for PCH DSW rails	ON	ON	ON	ON
+3VALW_PCH_PRIM	+3VALW power for PCH power rails	ON	ON	ON	ON*
+3VALW_SPI	+3VALW_PRIM supply for the SPI IO	ON	ON	ON	ON
+1.05VALW	+1.05V Always power rail	ON	ON	ON	ON
+1.2V_VDDQ	DDR4 +1.2V power rail	ON	ON	ON	OFF
+1.05V_VCCST	Sustain voltage for processor in Standby modes	ON	ON	OFF	OFF
+5VS	System +5V power rail	ON	OFF	OFF	OFF
+3VS	System +3V power rail	ON	OFF	OFF	OFF
+1.05VS_VCCSTG	+1.05VALW_PRIM Gated version of VCCST	ON	OFF	OFF	OFF
+0.6VS_VTT	DDR +0.6VS power rail for DDR terminator .	ON	OFF	OFF	OFF
+VCC_CORE	Core voltage for CPU	ON	OFF	OFF	OFF
+VCC_GT	Sliced graphics power rail	ON	OFF	OFF	OFF
+VCCIO	CPU IO +0.95VS power rail	ON	OFF	OFF	OFF
+VCC_SA	System Agent power rail	ON	OFF	OFF	OFF
+1.8VSDGPU_AON	+1.8VS power rail for GPU(AON rails)	ON	OFF	OFF	OFF
+1.8VSDGPU_MAIN	+1.8VS power rail for GPU GC6	ON	OFF	OFF	OFF
+VGA_CORE	Core voltage for VGA (merge core & core_s)	ON	OFF	OFF	OFF
+1.35VSDGPU	+1.35VS power rail for GPU	ON	OFF	OFF	OFF
+1.0VSDGPU	+1.0VS power rail for GPU	ON	OFF	OFF	OFF
+1.8VALW	System +1.8VALW always on power rail	ON	ON	ON	ON*

Note : ON\* means that this power plane is ON only with AC power available, otherwise it is OFF.

Board ID	PCB Revision	Board ID	PCB Revision
0	0.1	10	
1	1.0	11	1.0 w/ EC genso
2	1A	12	
3	1B	13	
4	1C	14	
5		15	
6		16	
7		17	
8		18	
9		19	



EH78F\_EVT Power Sequence

BIOS : 0.05

EC : 0.05

AC mode

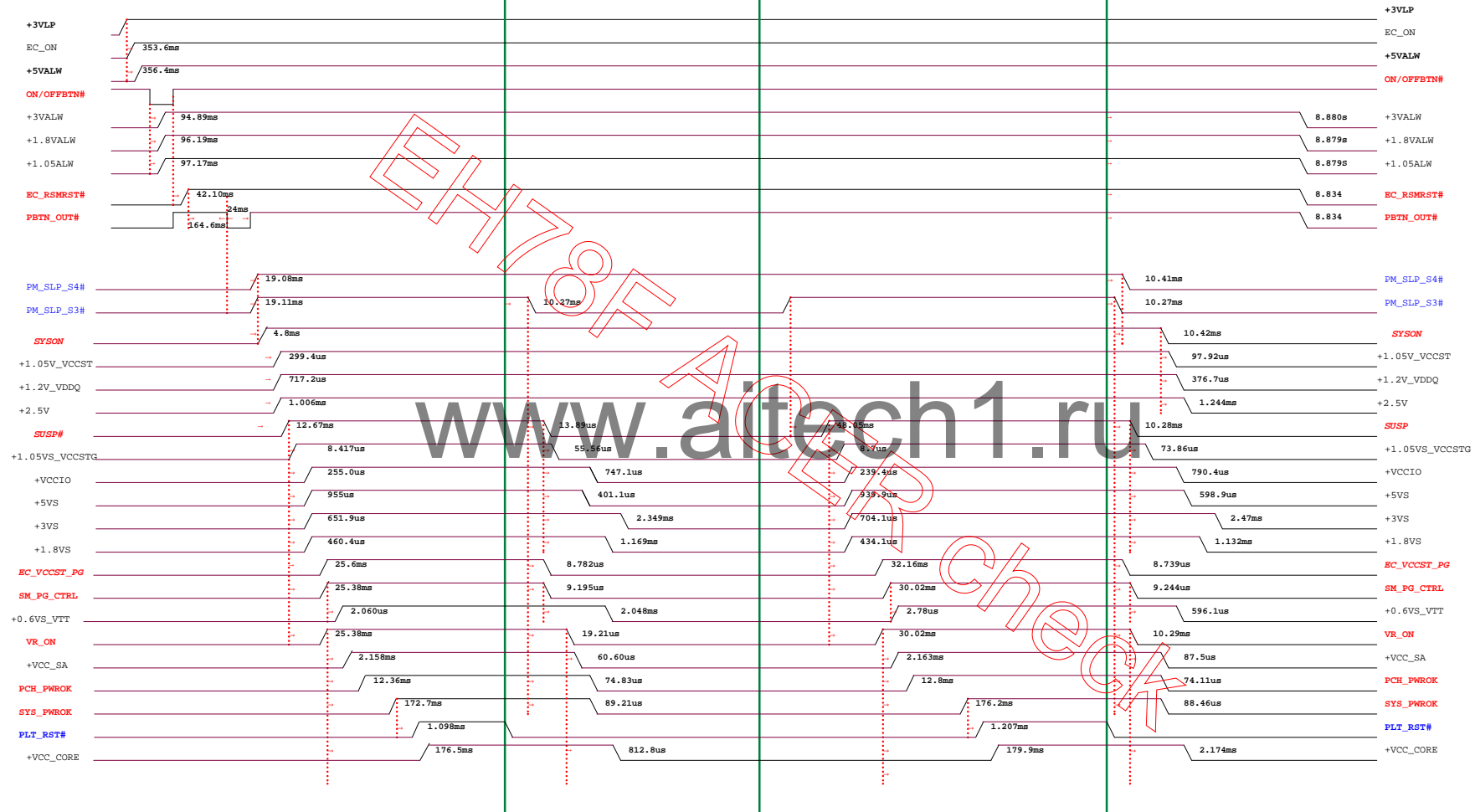
Plug in

Power On

S3

S3 Resume

Power Off



PCB DAZ

ZZZ

PCB@ DAZ2HB00100

PCB EH78F LA-G161P LS-G161P/G162P/G163P/G164P/G165P/G168P

Coffee Lake-H CPU SKU

UC1

CFL-H\_BGA1440

S IC CL8068403359524 SR3YY U0 2.2G ABO!

SA0000BPZ40

17@

Cannon Lake PCH SKU

UH1

CFL-H\_BGA1440

S IC FH82HM370 SR40B B0 BGA 874P PCH-H ABO!

SA0000BVP10

PCH@

NV N18E-G3

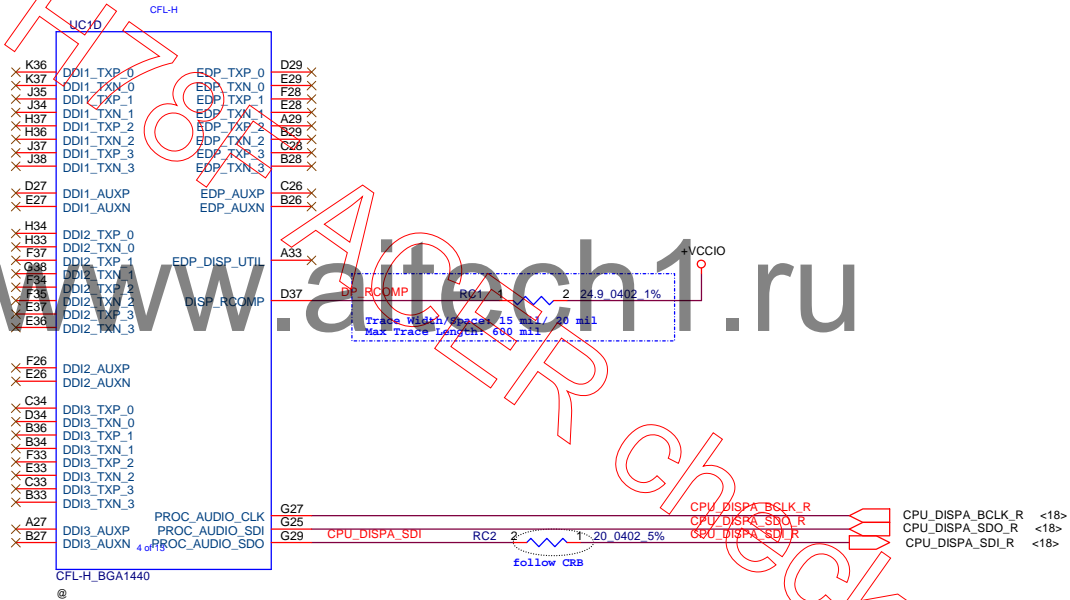
Need check USE QS PN

UG9

VGA@

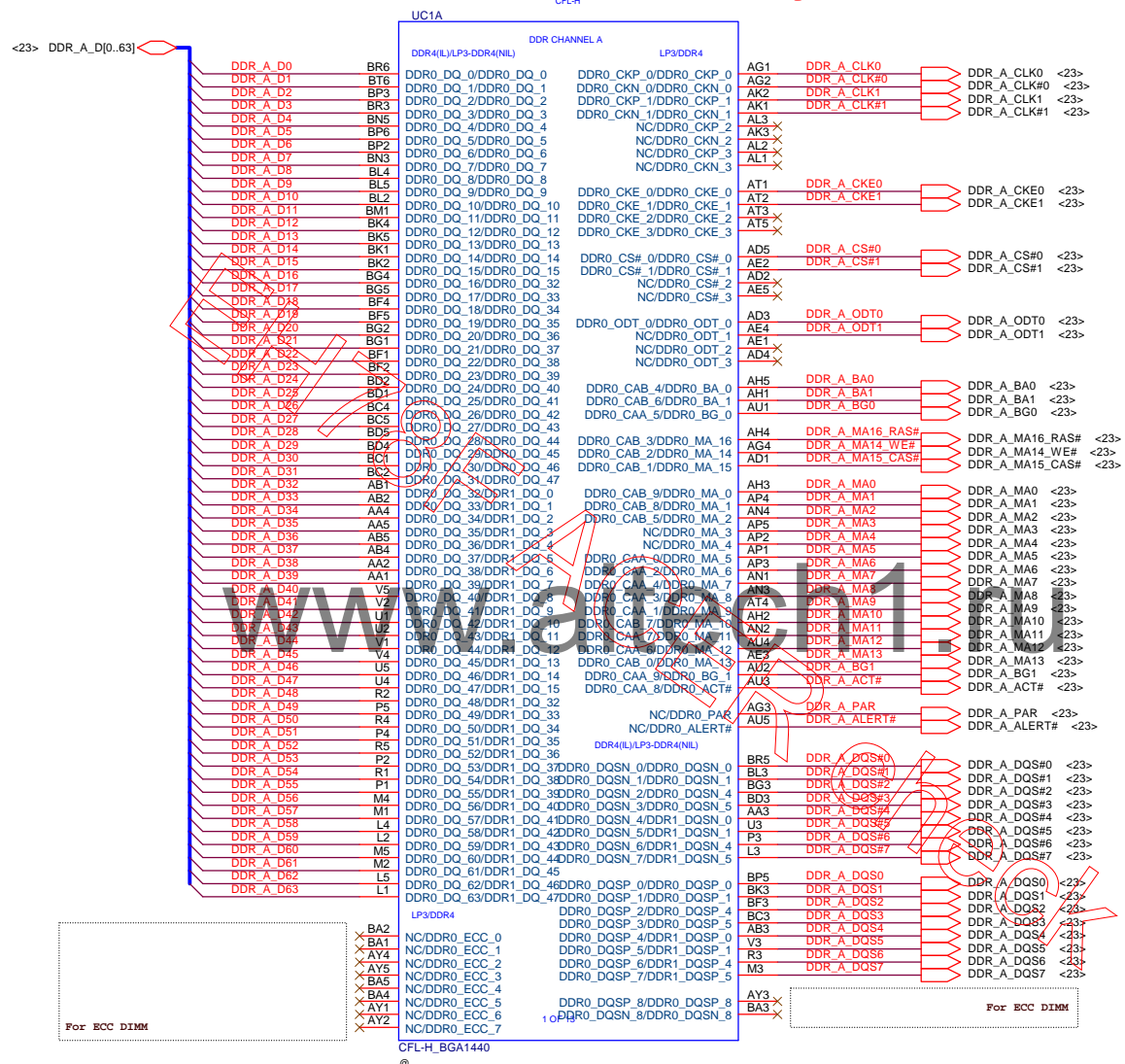
S IC TU104-750-A1 FCBGA 2228 GPU ABO !

SA0000CD510



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Issued Date		2017/11/23		CFL-H(1/8)DDI/eDP	
Deciphered Date		2018/09/01		Document Number	
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# Interleaved Memory



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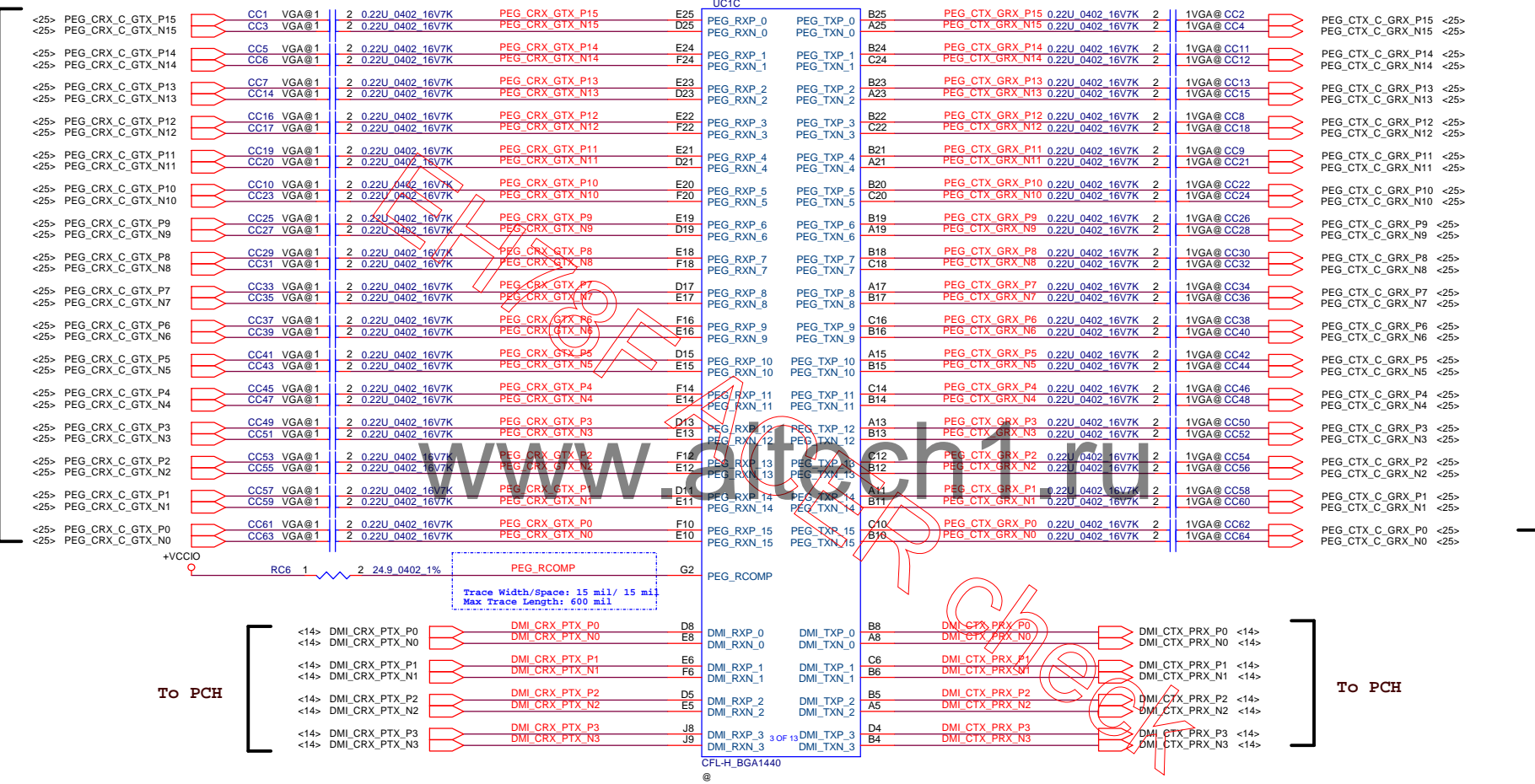
PEG&DMI

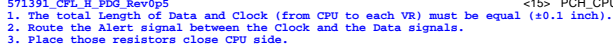
To DGPU  
PEG Lane Reversed

0806, chagne PEG AC cap to 0402 X7R

0806, chagne PEG AC cap to 0402 X7R

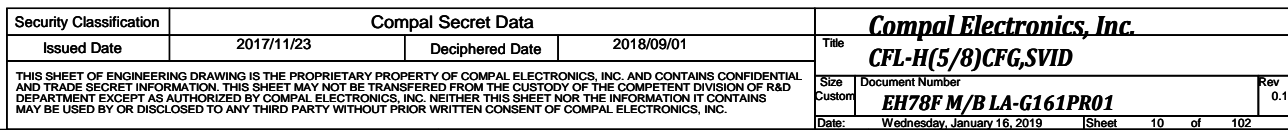
To DGPU  
PEG Lane Reversed

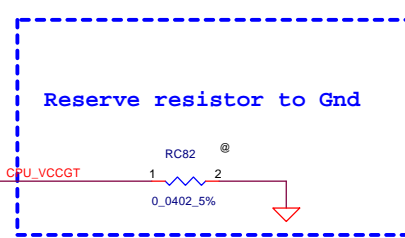




**Near CPU side**

follow 1050 Request  
8/21



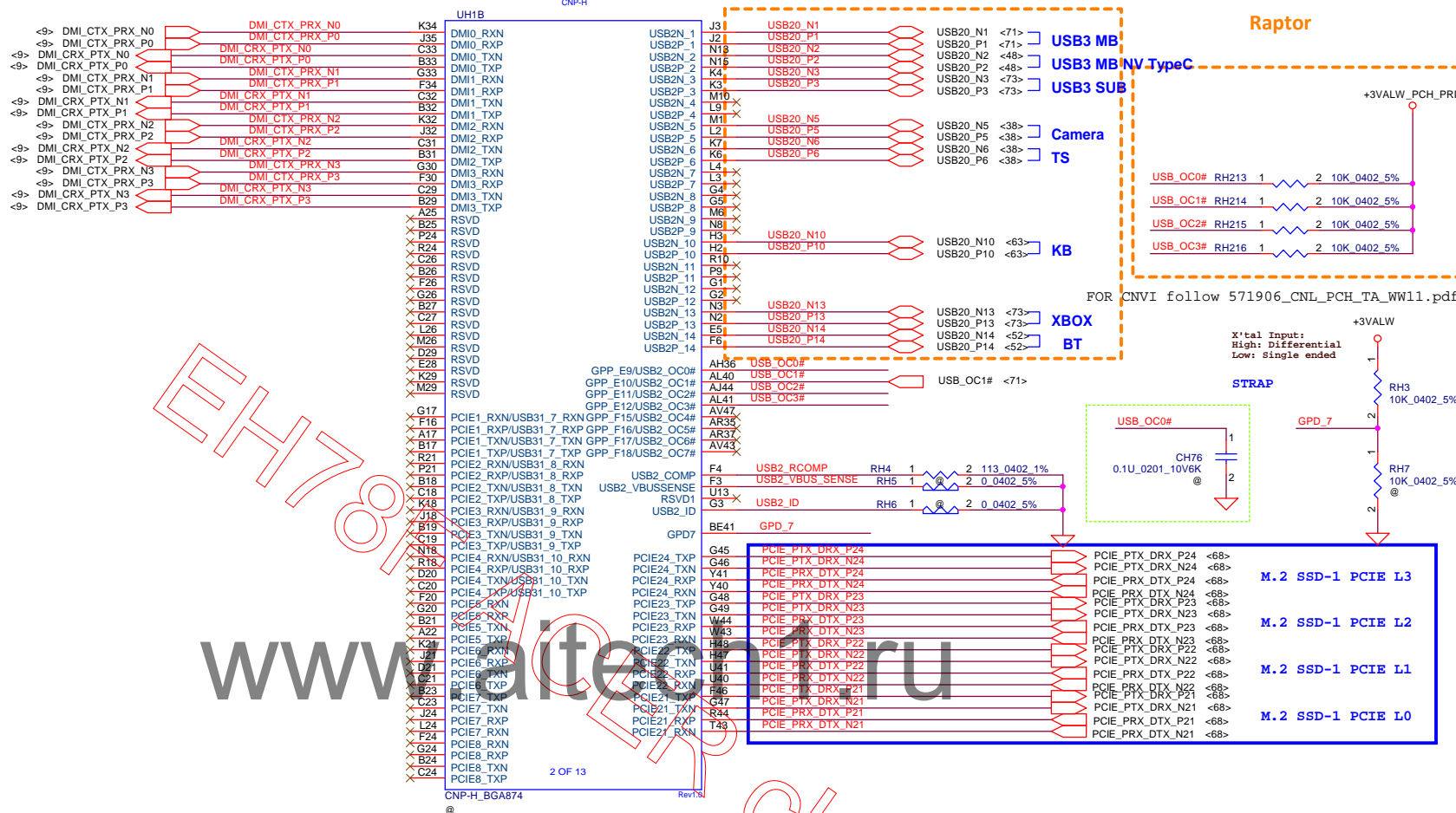


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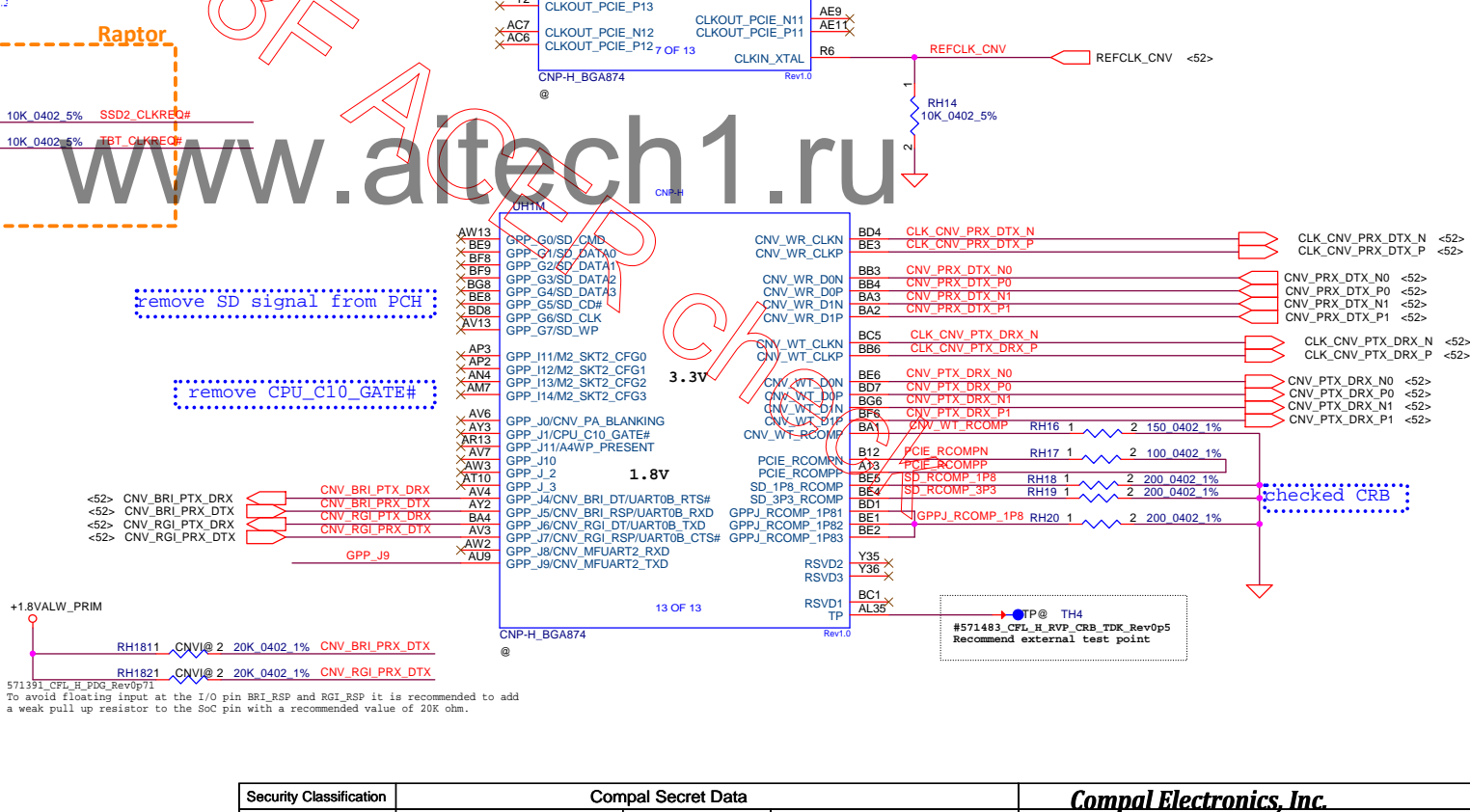
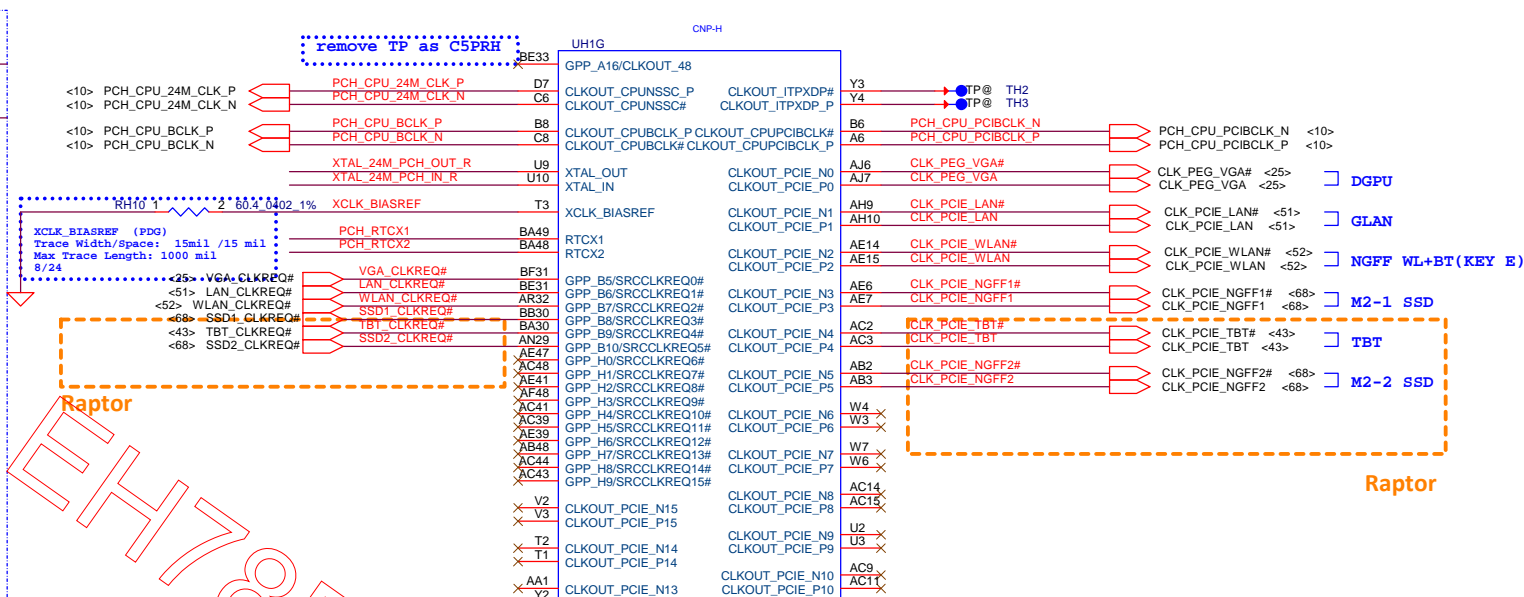


Flex I/O Lane	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29
High Speed I/O (HSIO) Type and Lane	USB3.1 #1	USB3.1 #2	USB3.1 #3	USB3.1 #4	USB3.1 #5	USB3.1 #6	USB3.1 #7	USB3.1 #8	USB3.1 #9	USB3.1 #10	PCIe* #5	PCIe* #6	PCIe* #7	PCIe* #8	PCIe* #9	PCIe* #10	PCIe* #11	PCIe* #12	PCIe* #13	PCIe* #14	PCIe* #15	PCIe* #16	PCIe* #17	PCIe* #18	PCIe* #19	PCIe* #20	PCIe* #21	PCIe* #22	PCIe* #23	PCIe* #24
							PCIe* #1		PCIe* #3	PCIe* #4		GbE			GbE		SATA 0a	SATA 1a	SATA 0b	SATA 1b	SATA 2	SATA 3	SATA 4	SATA 5						
Intel® RST Support						No Support					No Support					Yes			No Support					Yes			Yes			

The 30 HSIO lanes on PCH-H supports the following configurations:

- Up to 24 PCIe\* Lanes
  - A maximum of 16 PCIe\* Ports (or devices) can be enabled
  - When a GbE Port is enabled, the maximum number of PCIe\* Ports (or devices) that can be enabled reduces based off the following:
    - Max PCIe\* Ports (or devices) = 16 - GbE (0 or 1)
  - PCIe\* Lanes 1-4 (PCIe\* Controller #1), 5-8 (PCIe\* Controller #2), 9-12 (PCIe\* Controller #3), 13-16 (PCIe\* Controller #4), 17-20 (PCIe\* Controller #5), and 21-24 (PCIe\* Controller #6) can be individually configured
- Up to 6 SATA Lanes
  - A maximum of 6 SATA Ports (or devices) can be enabled
  - SATA Lane 0 has the flexibility to be mapped to Flex I/O Lane 16 or 18
  - SATA Lane 1 has the flexibility to be mapped to Flex I/O Lane 17 or 19
- Up to 10 USB 3.1 Lanes
  - A maximum of 10 USB 3.1 Ports (or devices) can be enabled
- Up to 4 GbE Lanes
  - A maximum of 1 GbE Port (or device) can be enabled
- Supports up to 3 Remapped (Intel® Rapid Storage Technology) PCIe\* storage devices
  - x2 and x4 PCIe\* NVMe SSD
  - x2 Intel® Optane® Memory Device
  - See the "PCI Express\* (PCIe\*)" chapter for the PCH PCIe\* Controllers, configurations, and lanes that can be used for Intel® Rapid Storage Technology PCIe\* storage support
- For unused SATA/PCIe\* Combo Lanes, Flex I/O Lanes that can be configured as PCIe\* or SATA, the lanes must be statically assigned to SATA or PCIe\* via the SATA/PCIe Combo Port Soft Straps discussed in the SPI Programming Guide and through the Intel® Flash Image Tool (FIT) tool.

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<39>	DP0_HPDP_PCH		RT881	1	Ⓢ	2	0	0402	5%
<40>	HDMI_HPDP_PCH								
<49>	CCG4_HOTPLUG_DET_3V3		RT880	1	Ⓢ	2	0	0402	5%
<42,43>	TBT_DP4_HPD		RT879	1	Ⓢ	2	0	0402	5%

```
.....remove PCH DP SCLK/SDATA
```

.....<51-58> FC PMF# [

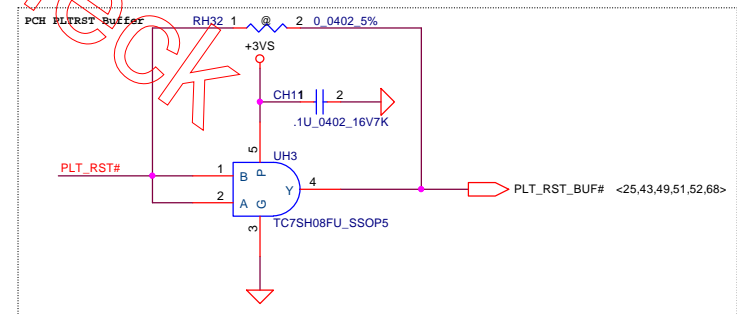
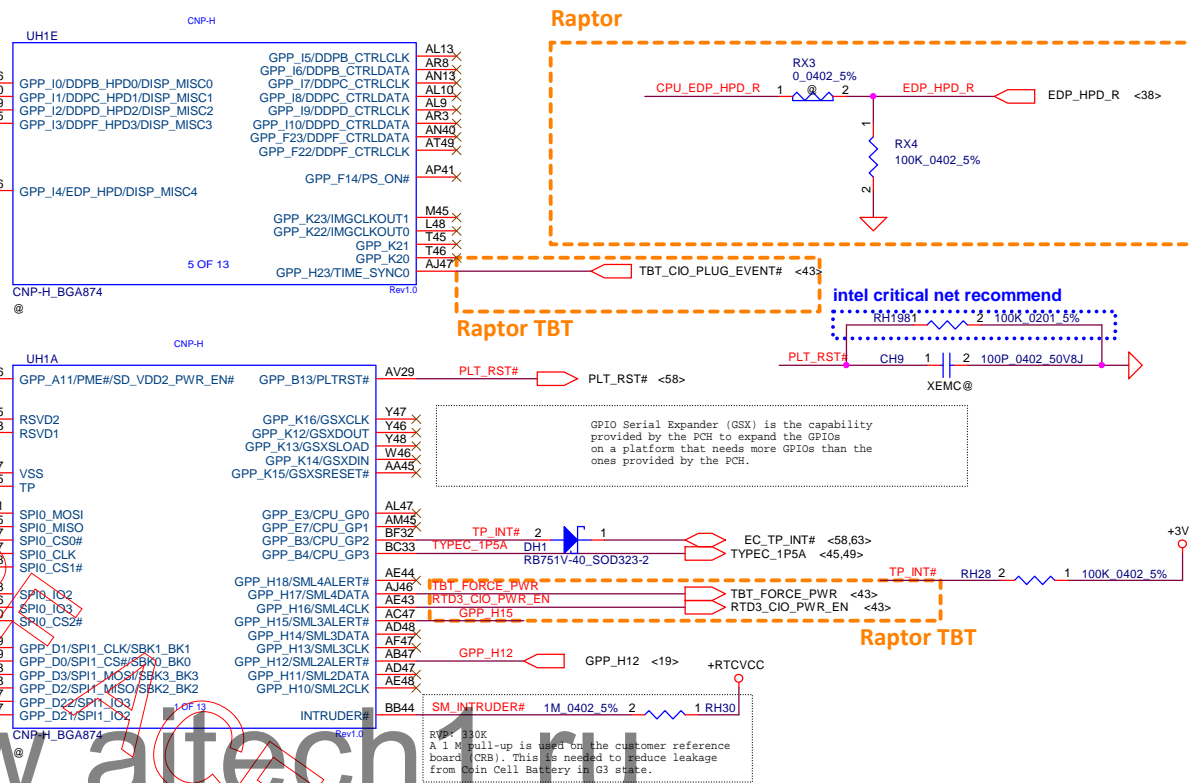
## Raptor

PCH\_SPI\_CLK RH1951 @ 2 100K\_0201\_5%

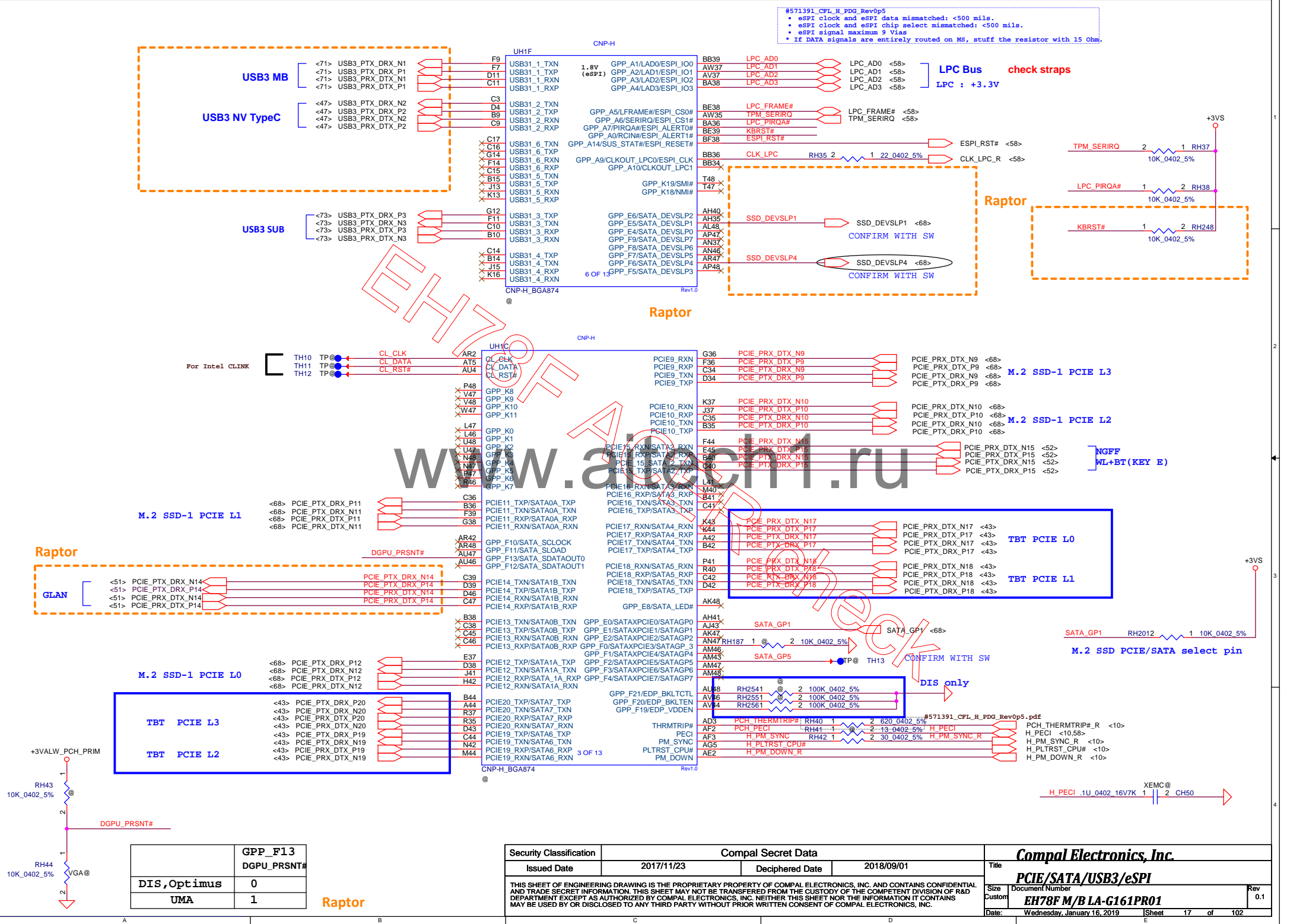
intel critical net recommend

[illegible]

intel PDG 1.8  
33 ohm for 3.3V for singel load  
place 500 mil from PCH



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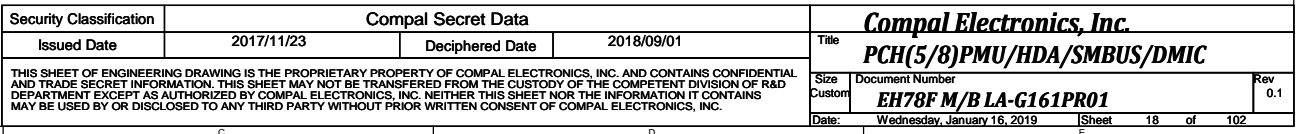


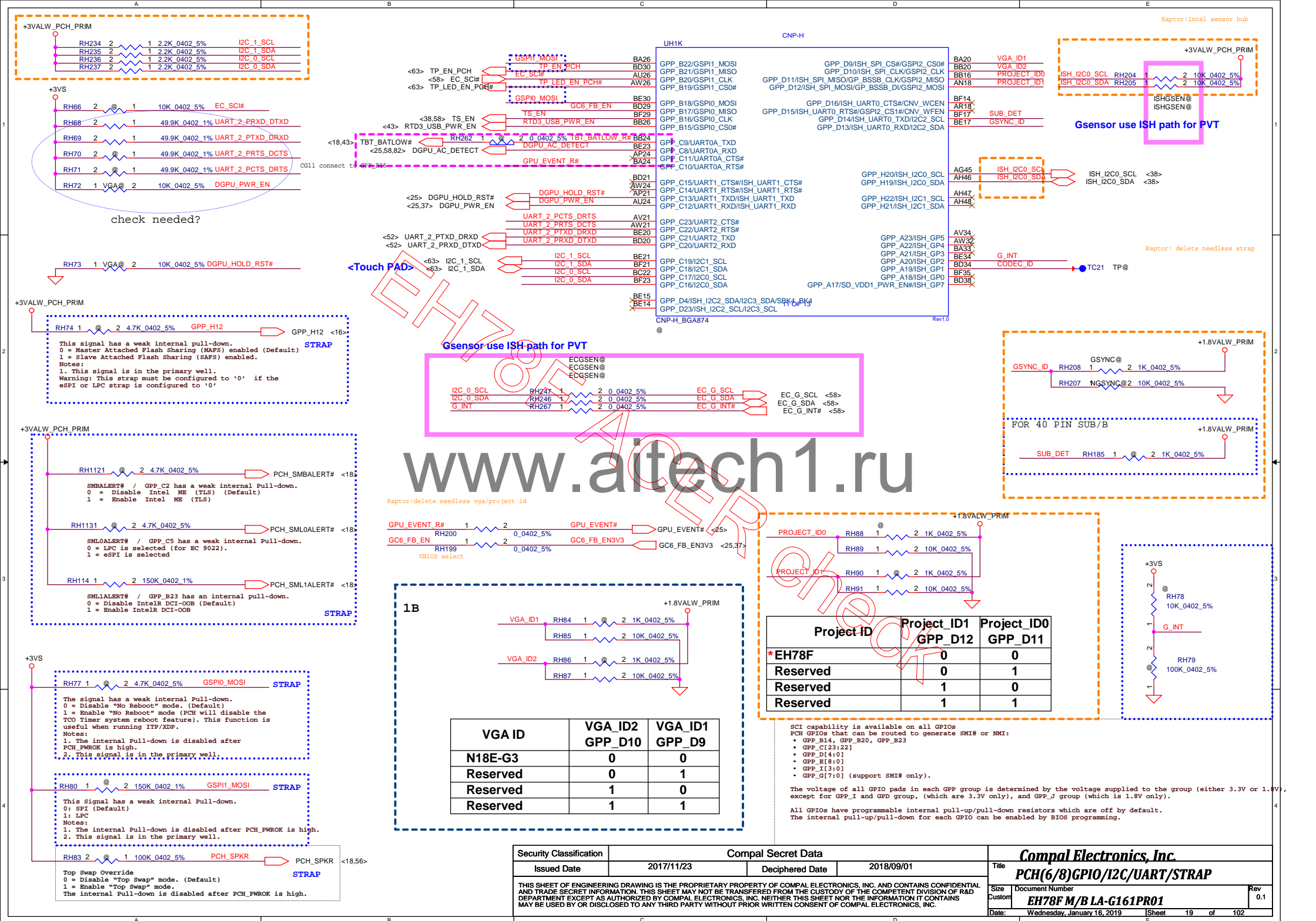
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	DGPU_PRSNT#
DIS,Optimus	0
UMA	1

Raptor

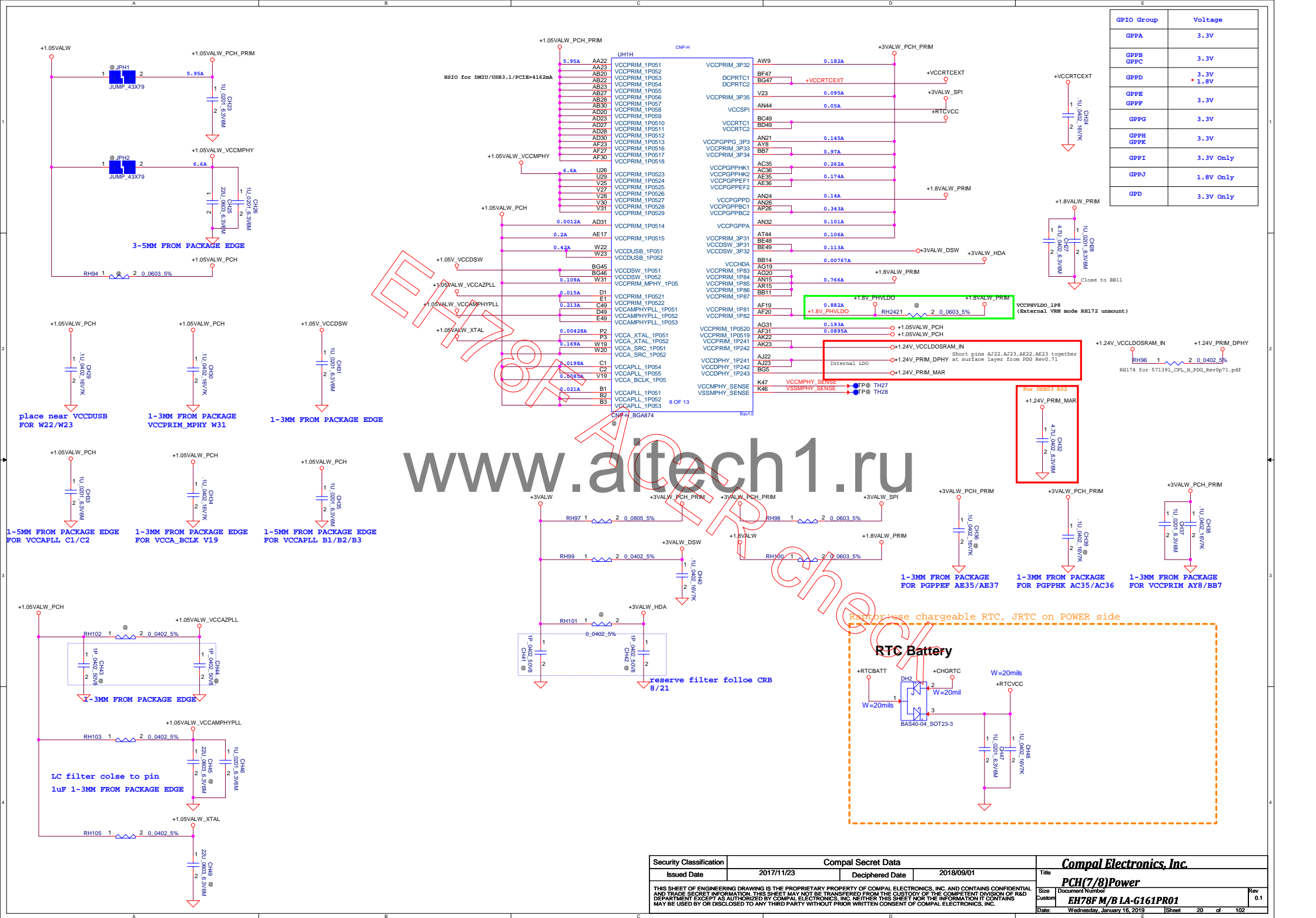
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Compal Electronics, Inc.	
PCIE/SATA/USB3/eSPI	
Size	Document Number
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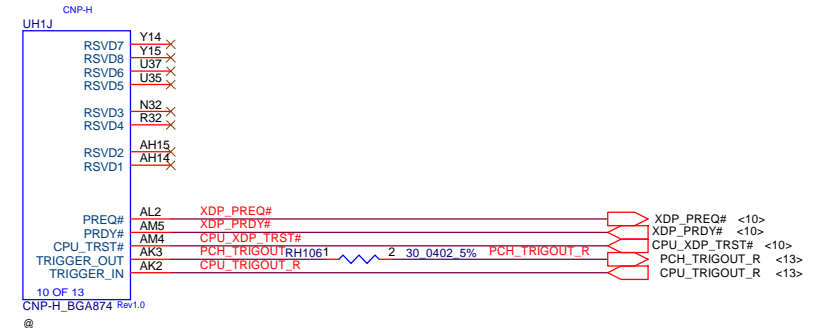
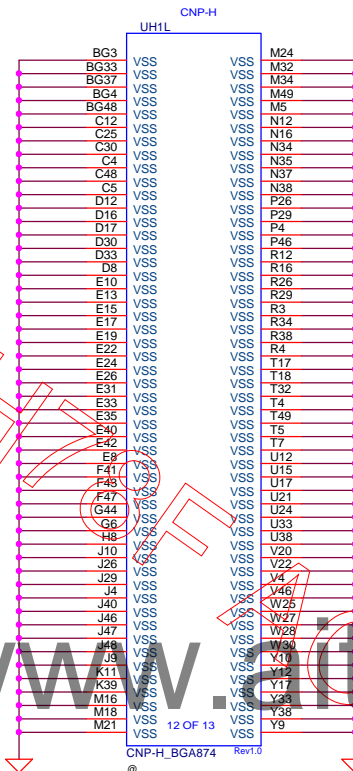
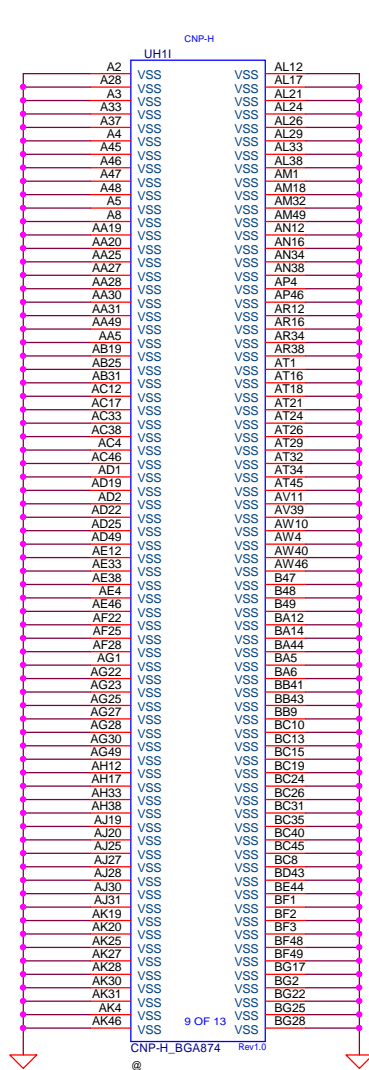






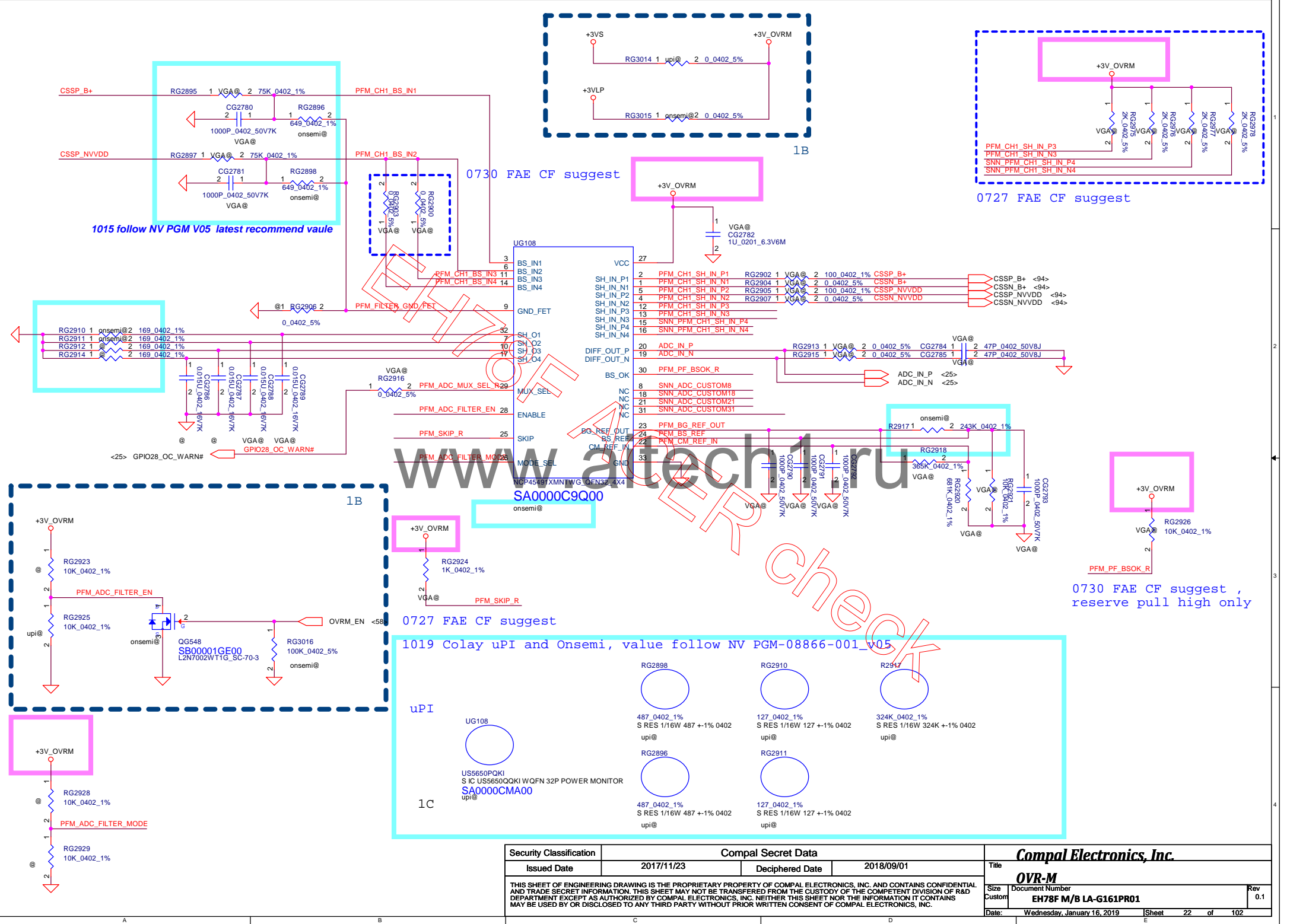


GPIO Group	Voltage
GPPA	3.3V
GPPB GPPC	3.3V
GPPD	3.3V + 1.8V
GPPE GPPF	3.3V
GPPG	3.3V
GPPH GPPK	3.3V
GPPI	3.3V Only
GPPJ	1.8V Only
GPD	3.3V Only



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										PCH(8/8)GND/RSVD	
										Size	
										Document Number	
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										Date	
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										21	
										of	
										102	
										Rev	
										0.1	

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				Date	Wednesday, January 16, 2019
				Sheet	22 of 102
				Rev	0.1

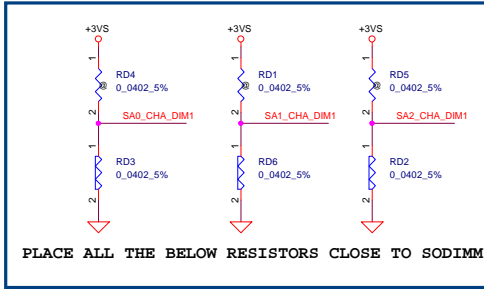


# CHANNEL-A

## TOP REVERSE (4mm)

### Interleaved Memory

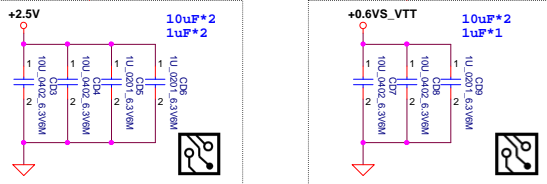
#### TOP: JDIMM1 CONN Non-ECC DIMM



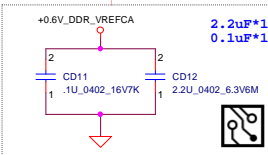
SPD ADDRESS FOR CHANNEL A :  
 WRITE ADDRESS: 0XA0  
 READ ADDRESS: 0XA1  
 SA0 = 0; SA1 = 0; SA2 = 0.  
 DDR4 POR OPERATING SPEED: 1867 MT/S  
 STRETCH GOAL IS 2133 MT/S

Layout Note:  
Place near JDIMM1.257,259

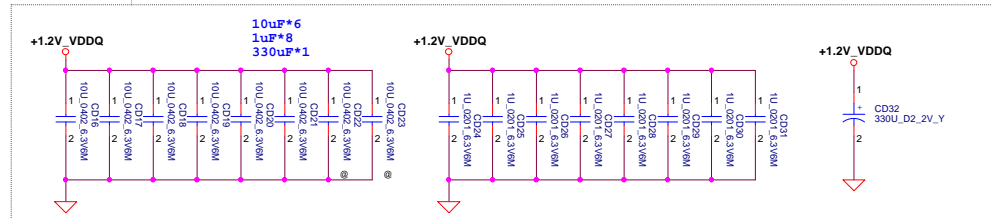
Layout Note:  
Place near JDIMM1.258



Layout Note:  
PLACE THE CAP near JDIMM1. 164

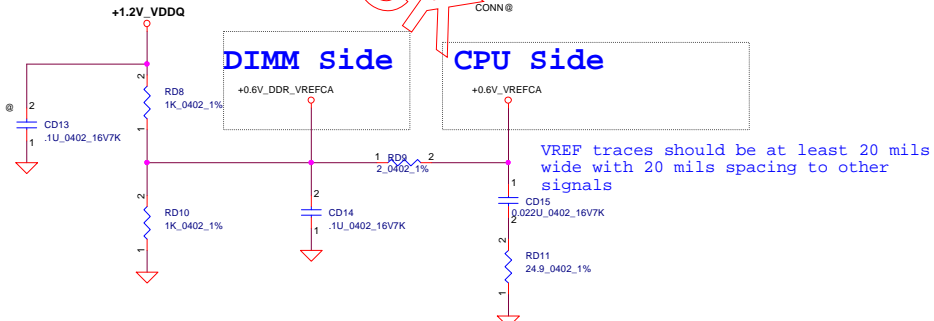
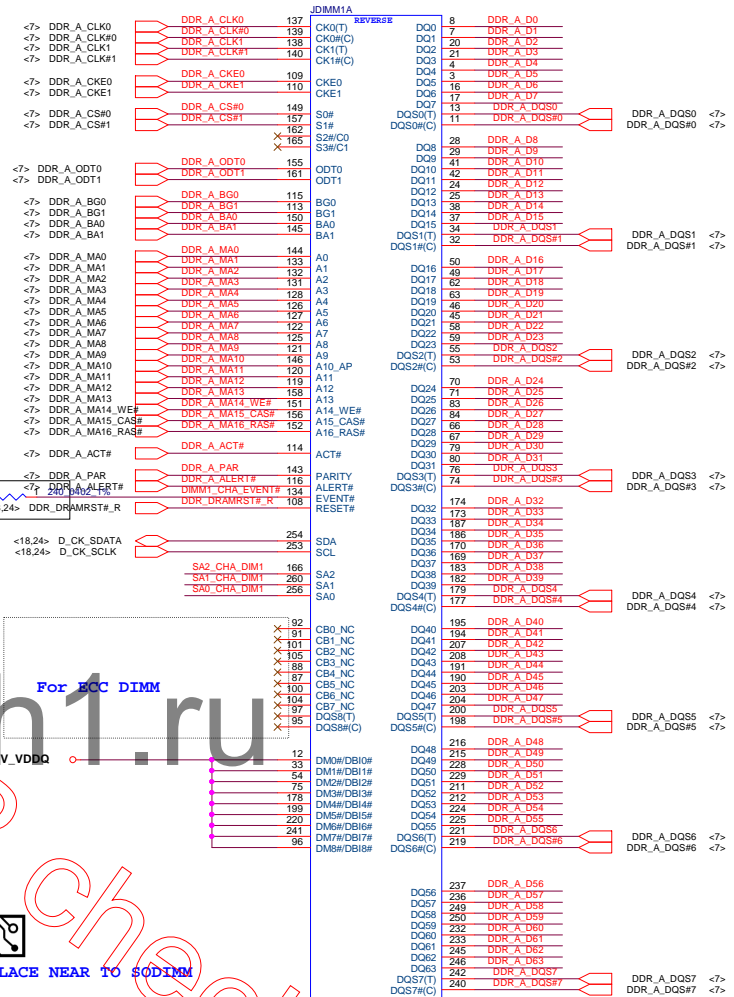


Layout Note:  
Place near JDIMM1



Part Number:SP07001CY00  
 Part Value:S SOCKET LOTES ADDR0206-P001A 260P DDR4

Connector follow 2018V-VX



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Issued Date	2017/11/23	Deciphered Date	2018/09/01			Title	DDRIV_CHA: DIMM0	
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						Date:	Wednesday, January 16, 2019	Sheet 23 of 102

## TOP REV (8mm) Interleaved Memory

```
SPD ADDRESS FOR CHANNEL B :
WRITE ADDRESS: 0XA4
READ ADDRESS: 0XA3
SA0 = 0; SA1 = 1; SA2 = 0.
DDR4 POR OPERATING SPEED: 1867 MT/S
STRETCH GOAL IS 2133 MT/S
```

Layout Note:  
Place near JDIMM2.258

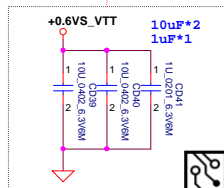
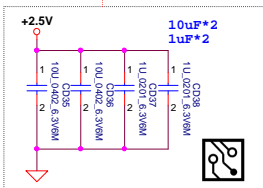
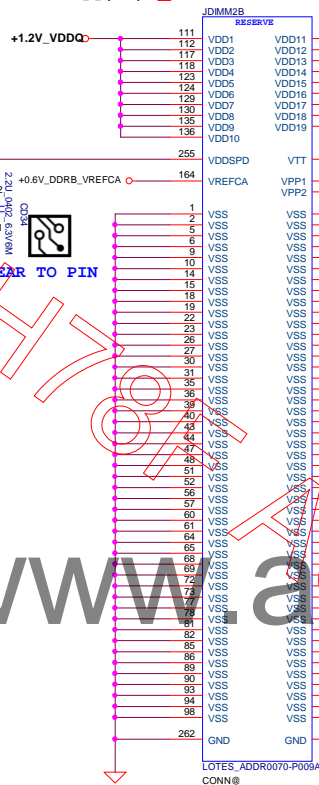
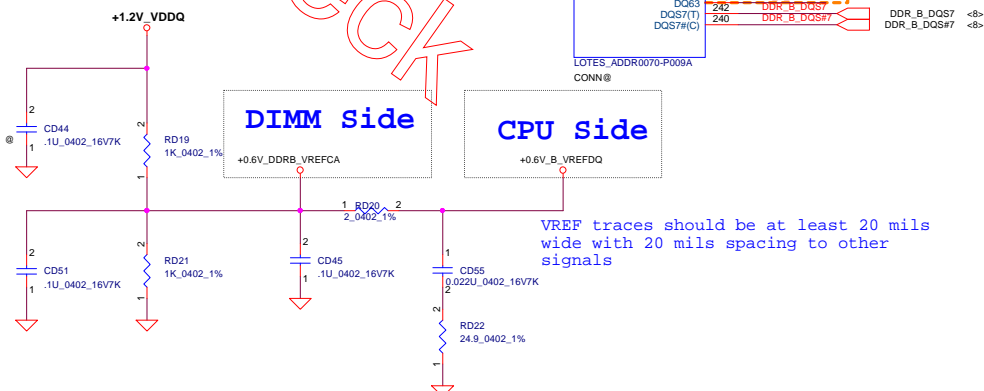


Figure 10 shows two schematic diagrams of the input and output buffers for the 100-pin package. The left diagram is the input buffer, and the right diagram is the output buffer. Both are powered by +1.2V VDDQ. The input buffer (left) shows a 100-ohm series resistor and a 100-pF shunt capacitor to ground. The output buffer (right) shows a 100-ohm series resistor and a 100-pF shunt capacitor to ground. The components are labeled as follows:

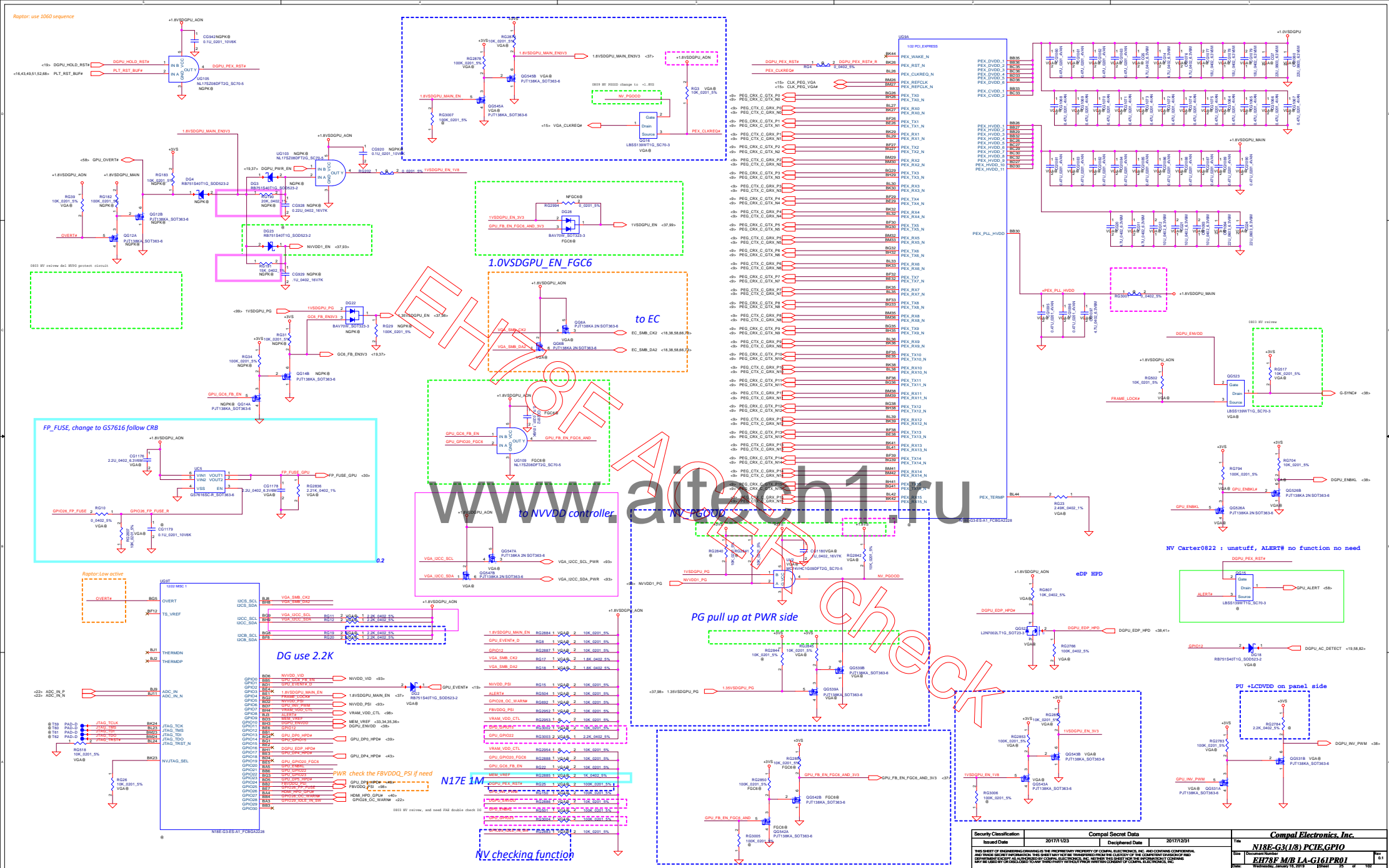
- Input Buffer (Left): CD54, CD55, CD56, CD57, CD58, CD59, CD60, CD61, CD62, CD63, CD64.
- Output Buffer (Right): CD65, CD66, CD67, CD68, CD69, CD70, CD71, CD72, CD73, CD74, CD75, CD76, CD77, CD78, CD79, CD80, CD81, CD82, CD83, CD84, CD85, CD86, CD87, CD88, CD89, CD90, CD91, CD92, CD93, CD94, CD95, CD96, CD97, CD98, CD99, CD100.



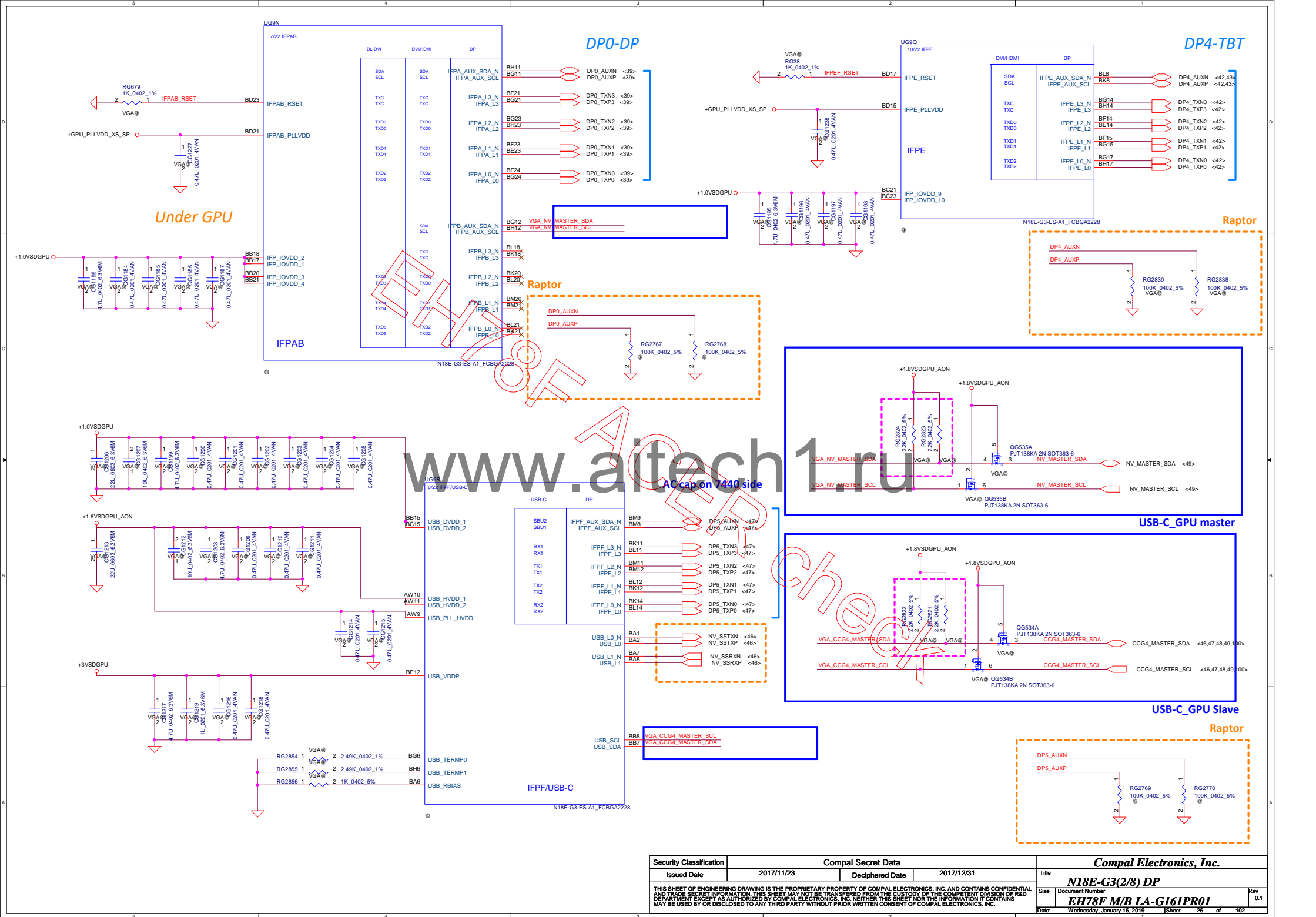
Connector follow 2018V-VX



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						Size
						EH78F M/B LA-G161PRO1
Date: Wednesday, January 16, 2019						Sheet 24 of 102

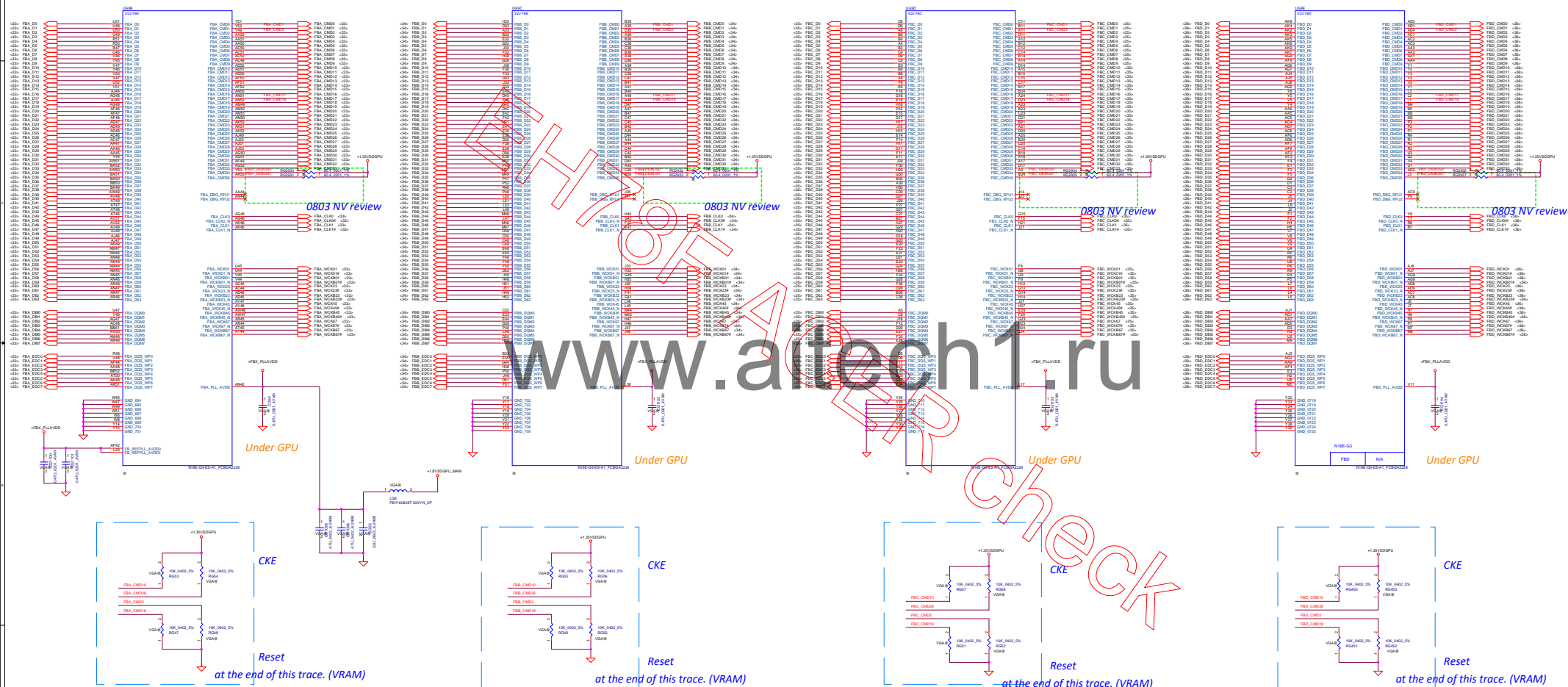


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Ym		Compal Electronics, Inc.	
N18E-G3(1/8) PCIE.GPIO		N18E-G3(1/8) PCIE.GPIO	
Rev		Rev	
EH78F M/LA-G161PRO1		EH78F M/LA-G161PRO1	
Date		Date	
Wednesday, January 18, 2017		2017/1/18	













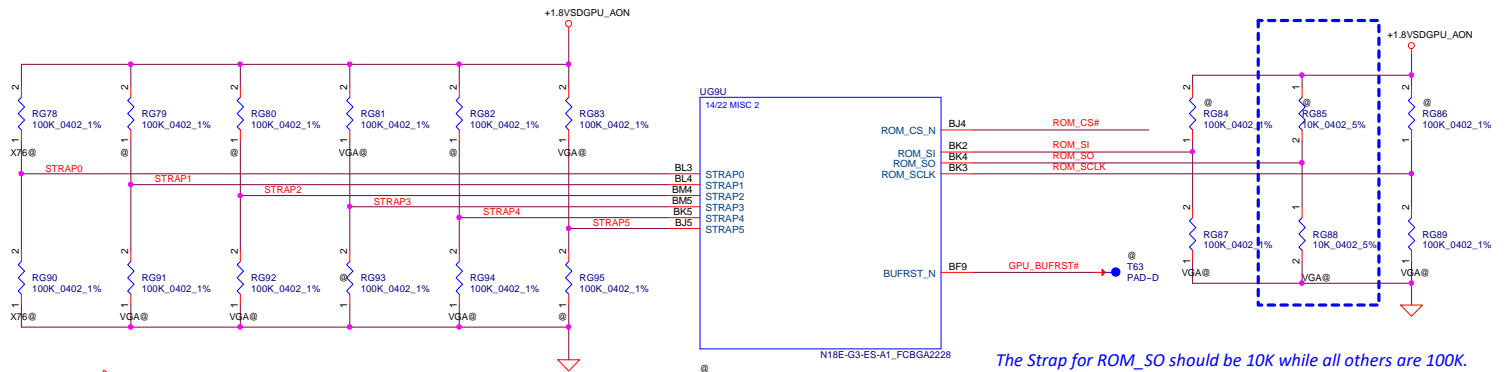


	(LSB)	(MSB)	(LSB)	(MSB)					
<b>G-sync with VGA device</b>	Strap0	Strap1	Strap2	Strap3	Strap4	Strap5	ROM_SO	ROM_SI	ROM_SCLK
<b>MICRON</b> MT61K256M32JE-14:A	PU 100kOhm	PD 100kOhm	PD 100kOhm	PU 100kOhm	PD 100kOhm	PU 100kOhm	PD 10kOhm	PD 100kOhm	PD 100kOhm
<b>Samsung</b> K4Z80325BC-HC14	PD 100kOhm	PD 100kOhm	PD 100kOhm	PU 100kOhm	PD 100kOhm	PU 100kOhm	PD 10kOhm	PD 100kOhm	PD 100kOhm

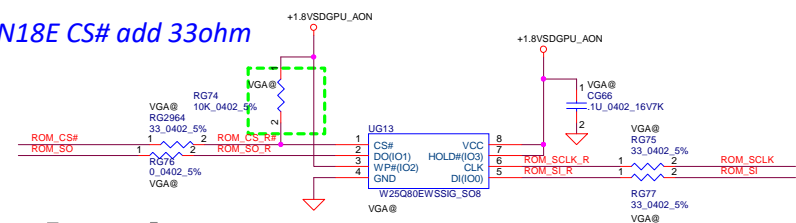
Table 1. N18E-G3 GDDR6 Recommended Memories

Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code	Alert	Qual Plan	Status
8 Gb	2Chx256Mx16	1.25V and 1.35V <sup>2</sup>	Micron	MT61K256M32JE-14:A	A-die	0x1	14 Gbps	N/A		Full	Production candidate
			Samsung	K4Z80325BC-HC14	C-die	0x0	14 Gbps	N/A		Full	Production candidate

Notes:  
1. For N18E-G3, the maximum allowable memory case temperature is 95 °C.  
2. DVS is required. WCK: TBD



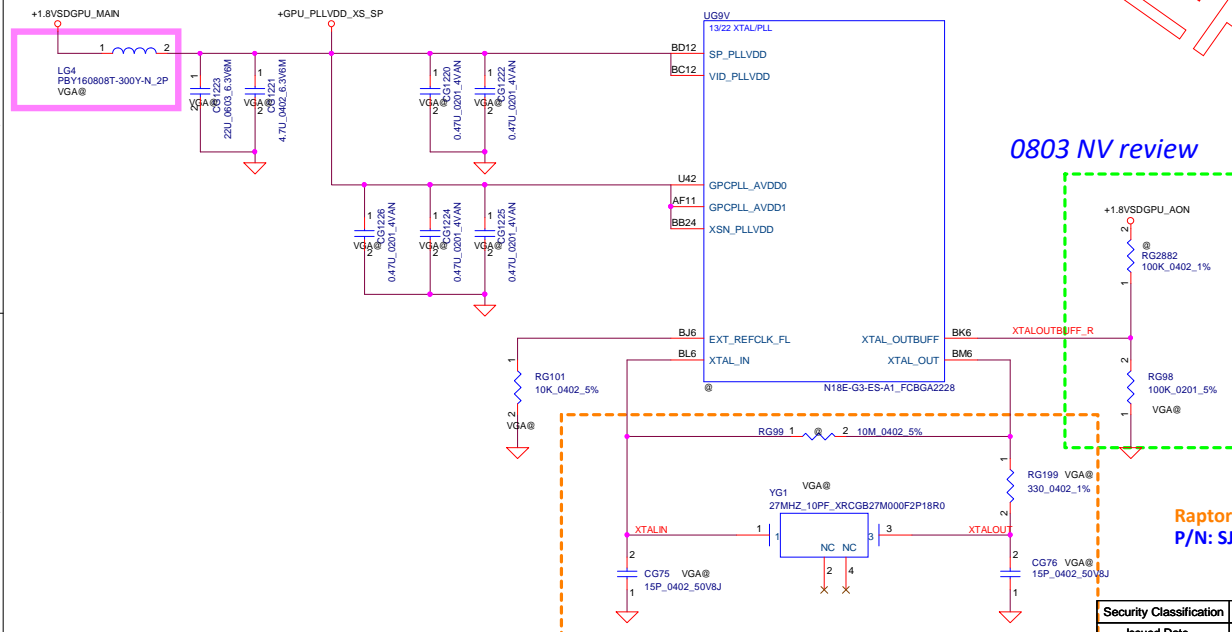
N18E CS# add 33ohm



DGPU VBIOS ROM 8Mb

www.aitech1.ru

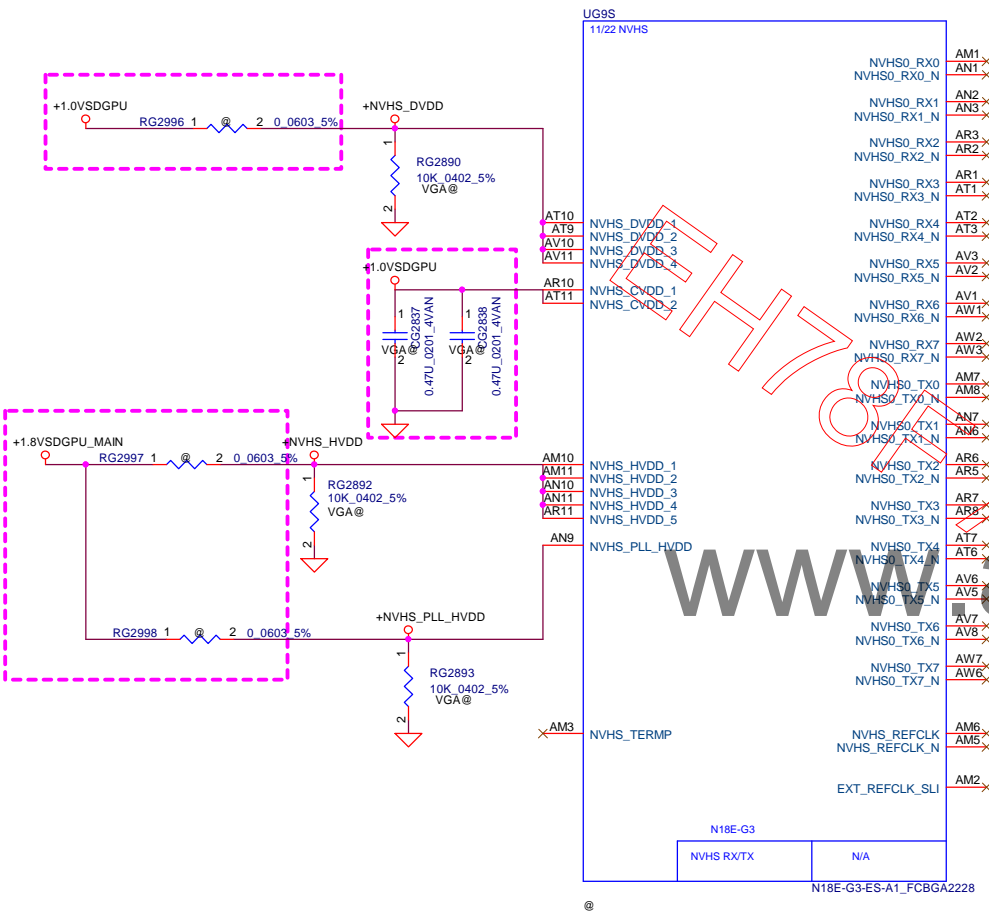
0803 NV review



Raptor: change to follow 2018 VX SJ10000UI00  
P/N: SJ10000UI00 (S CRYSTAL 27MHZ 10PF XRCGB27M000F2P18R0)

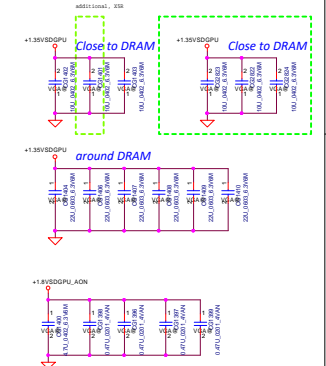
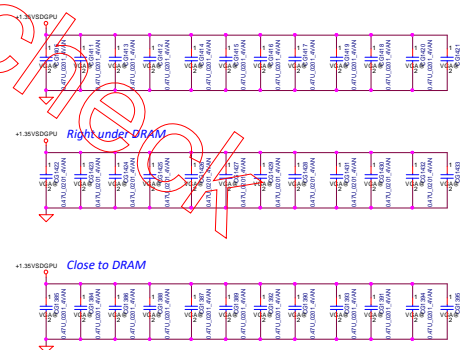
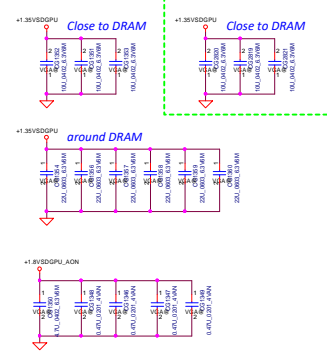
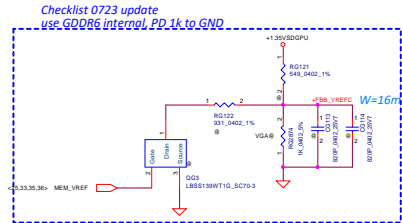
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Issued Date	2017/11/23	Deciphered Date	2017/12/31	Title	N18E-G3(7/8) Strap,ROM
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				Part Number	EH78F M/B LA-G161PR01

Pull down NVHS\_DVDD, NVHS\_CVDD, NVHS\_HVDD, NVHS\_PLL\_HVDD rails to GND with 10K Resistor



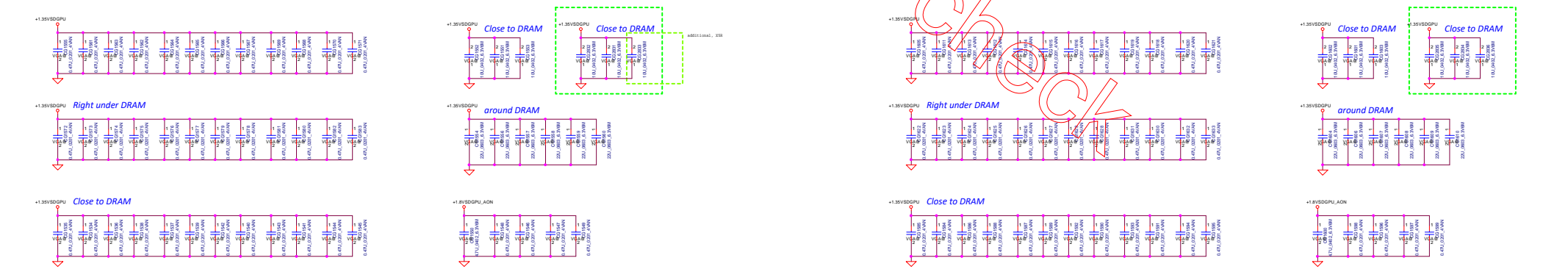
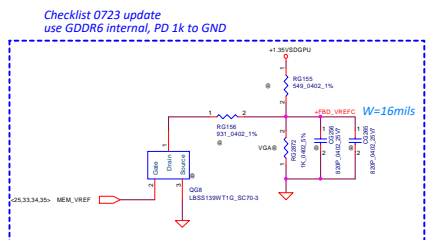
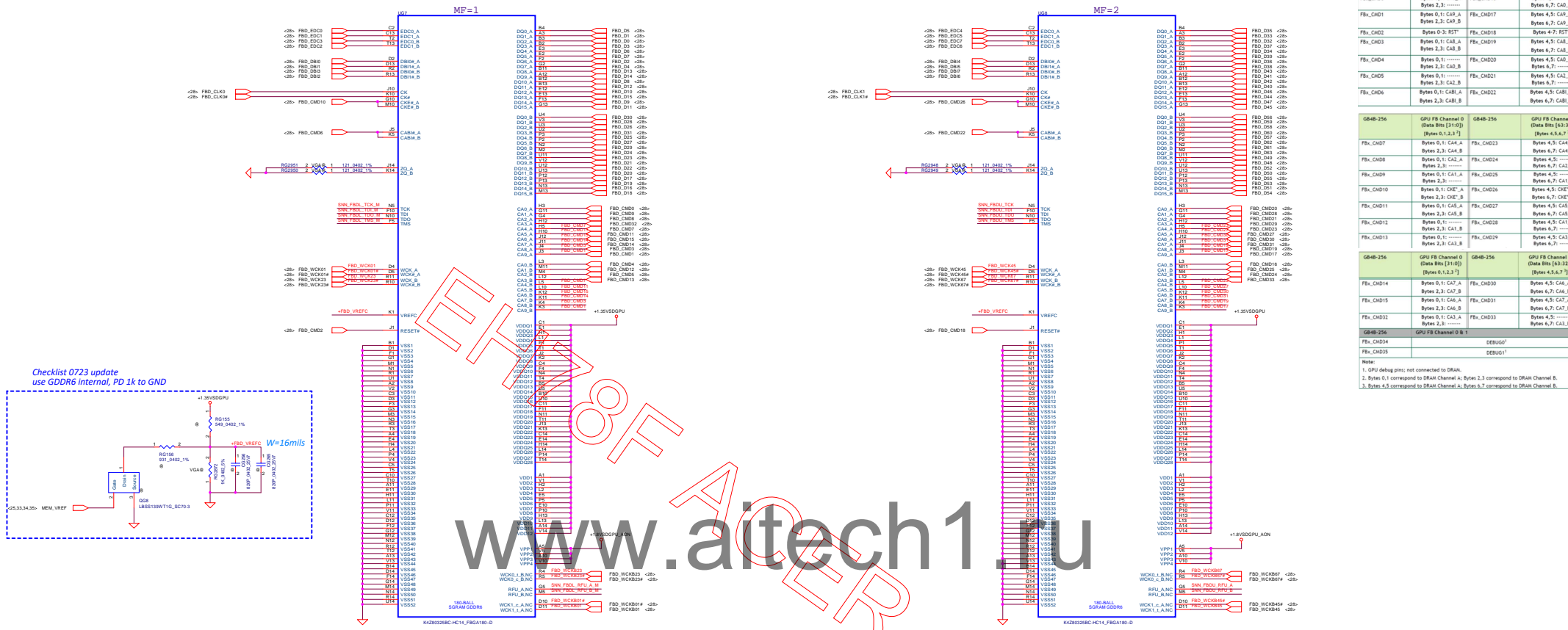
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2017/11/23		2017/12/31		Title	
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Size		Document Number		0.1	
Date		Wednesday, January 16, 2019		Sheet	
32		of		102	











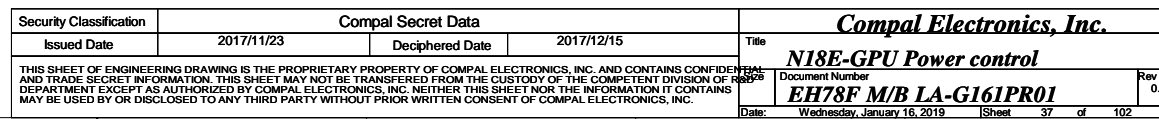
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Fb_C4D0	Bytes 0,1: C4D_A Bytes 2,3: C4D_B	Fb_C4D16	Bytes 4,5: C4D_A Bytes 6,7: C4D_B
Fb_C4D1	Bytes 0,1: C4D_A Bytes 2,3: C4D_B	Fb_C4D17	Bytes 4,5: C4D_A Bytes 6,7: C4D_B
Fb_C4D2	Bytes 0,1: RST Bytes 2,3: C4D_B	Fb_C4D18	Bytes 4,5: C4D_A Bytes 6,7: C4D_B
Fb_C4D3	Bytes 0,1: C4D_A Bytes 2,3: C4D_B	Fb_C4D19	Bytes 4,5: C4D_A Bytes 6,7: C4D_B
Fb_C4D4	Bytes 0,1: C4D_A Bytes 2,3: C4D_B	Fb_C4D20	Bytes 4,5: C4D_A Bytes 6,7: C4D_B
Fb_C4D5	Bytes 0,1: C4D_A Bytes 2,3: C4D_B	Fb_C4D21	Bytes 4,5: C4D_A Bytes 6,7: C4D_B
Fb_C4D6	Bytes 0,1: C4D_A Bytes 2,3: C4D_B	Fb_C4D22	Bytes 4,5: C4D_A Bytes 6,7: C4D_B

GB4B-256	GPU FB Channel 0 (Data Bits [31:0]) (Bytes 0.1,3,7)	GB4B-256	GPU FB Channel 1 (Data Bits [31:0]) (Bytes 4.5,6,7)
Fb_C4D7	Bytes 0,1: C4D_A Bytes 2,3: C4D_B	Fb_C4D23	Bytes 4,5: C4D_A Bytes 6,7: C4D_B
Fb_C4D8	Bytes 0,1: C4D_A Bytes 2,3: C4D_B	Fb_C4D24	Bytes 4,5: C4D_A Bytes 6,7: C4D_B
Fb_C4D9	Bytes 0,1: C4D_A Bytes 2,3: C4D_B	Fb_C4D25	Bytes 4,5: C4D_A Bytes 6,7: C4D_B
Fb_C4D10	Bytes 0,1: C4D_A Bytes 2,3: C4D_B	Fb_C4D26	Bytes 4,5: C4D_A Bytes 6,7: C4D_B
Fb_C4D11	Bytes 0,1: C4D_A Bytes 2,3: C4D_B	Fb_C4D27	Bytes 4,5: C4D_A Bytes 6,7: C4D_B
Fb_C4D12	Bytes 0,1: C4D_A Bytes 2,3: C4D_B	Fb_C4D28	Bytes 4,5: C4D_A Bytes 6,7: C4D_B
Fb_C4D13	Bytes 0,1: C4D_A Bytes 2,3: C4D_B	Fb_C4D29	Bytes 4,5: C4D_A Bytes 6,7: C4D_B

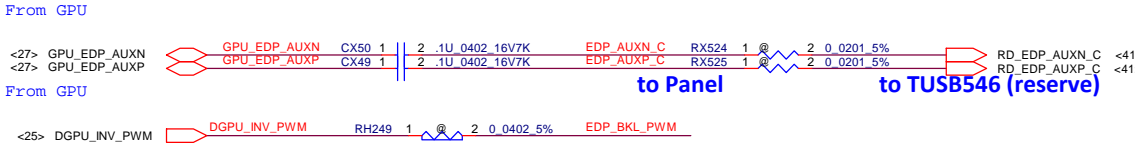
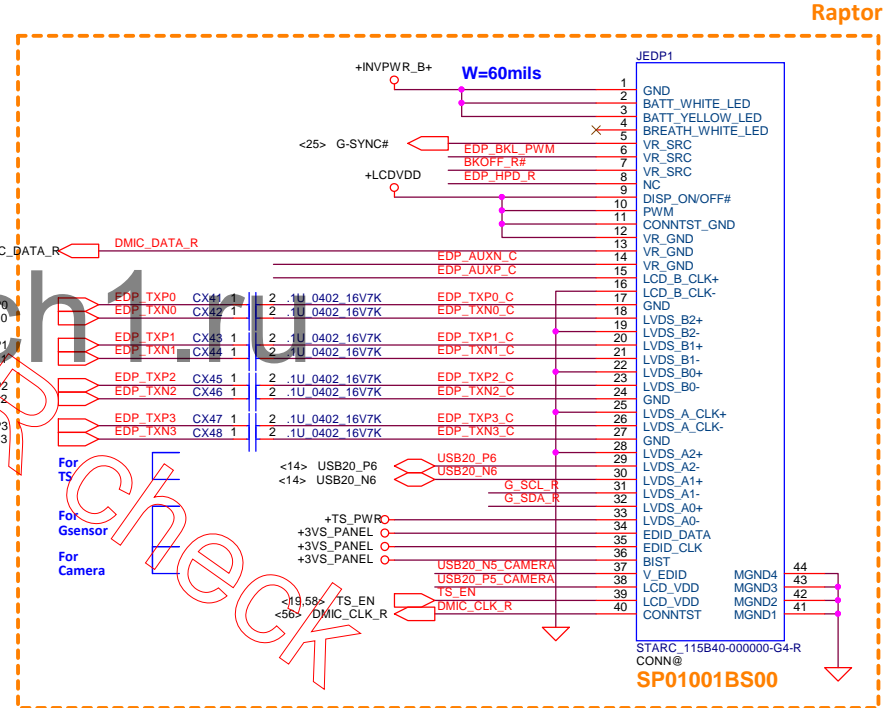
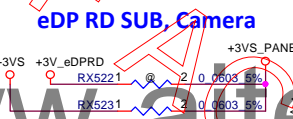
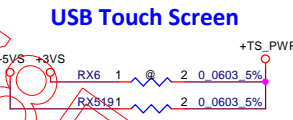
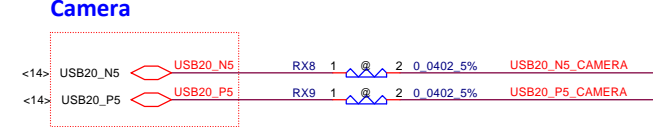
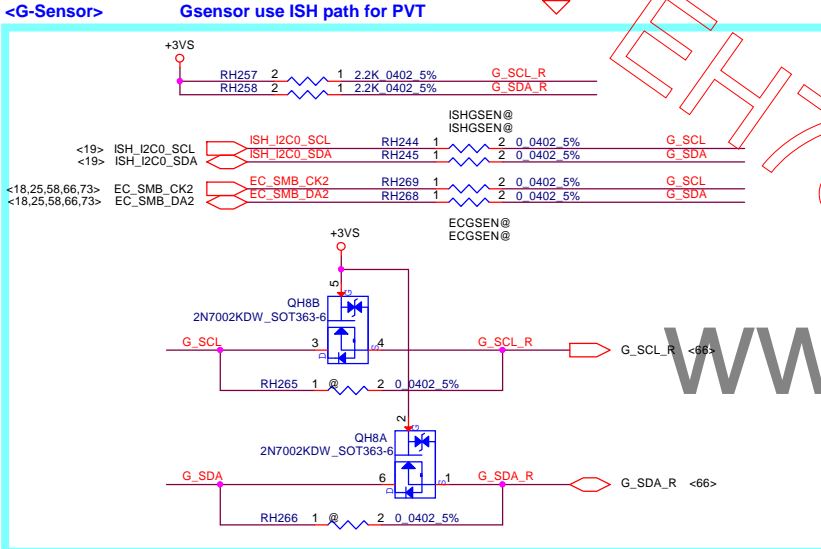
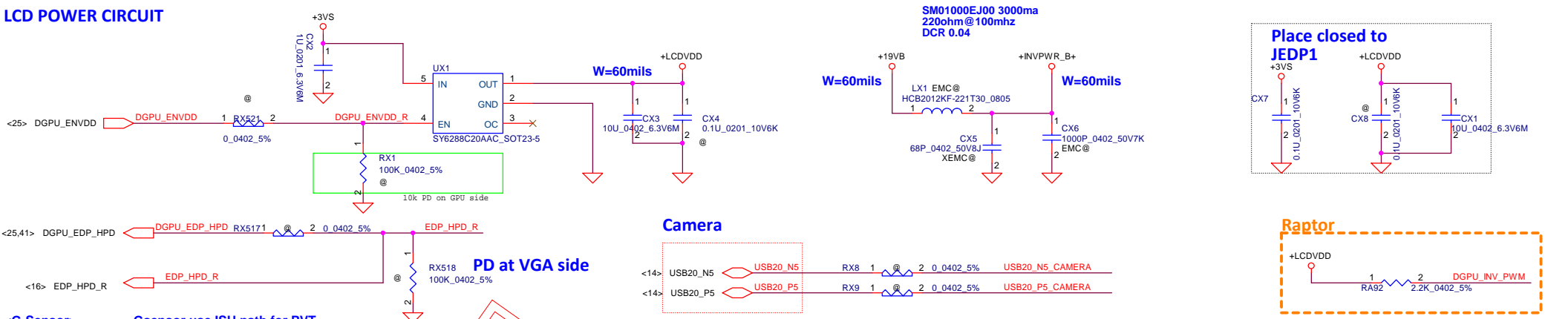
GB4B-256	GPU FB Channel 0 (Data Bits [31:0]) (Bytes 0.1,3,7)	GB4B-256	GPU FB Channel 1 (Data Bits [31:0]) (Bytes 4.5,6,7)
Fb_C4D14	Bytes 0,1: C4D_A Bytes 2,3: C4D_B	Fb_C4D30	Bytes 4,5: C4D_A Bytes 6,7: C4D_B
Fb_C4D15	Bytes 0,1: C4D_A Bytes 2,3: C4D_B	Fb_C4D31	Bytes 4,5: C4D_A Bytes 6,7: C4D_B
Fb_C4D16	Bytes 0,1: C4D_A Bytes 2,3: C4D_B	Fb_C4D32	Bytes 4,5: C4D_A Bytes 6,7: C4D_B

Notes:  
1. GPU debug pins: not connected to DRAM.  
2. Bytes 0,1 correspond to DRAM Channel A; Bytes 2,3 correspond to DRAM Channel B.  
3. Bytes 4,5 correspond to DRAM Channel A; Bytes 6,7 correspond to DRAM Channel B.

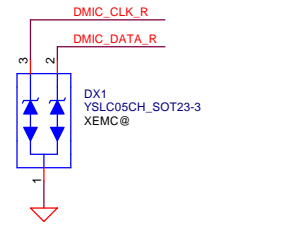
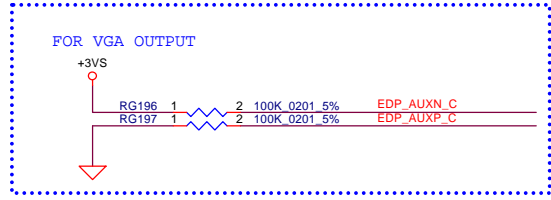
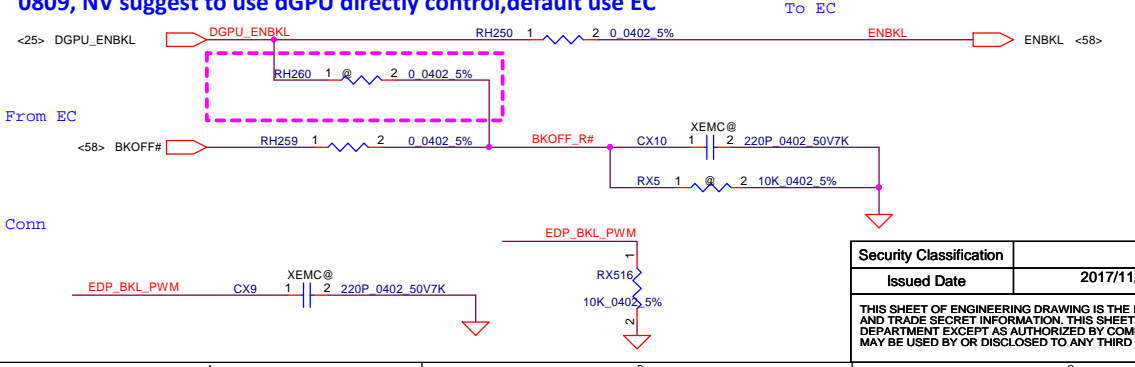
## +1.8VALW to +1.8VSDGPU\_AON & +3VS to +3VSDGPU



LCD POWER CIRCUIT

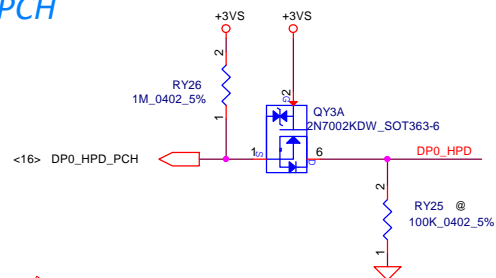


0809, NV suggest to use dGPU directly control,default use EC

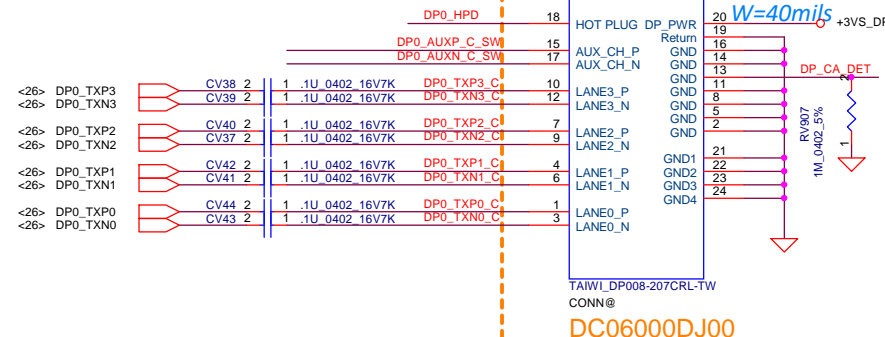


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				Custom	EH78F M/B LA-G161PR01
				Date	Wednesday, January 16, 2019
				Sheet	38 of 102
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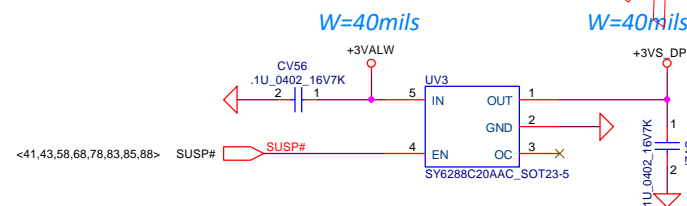
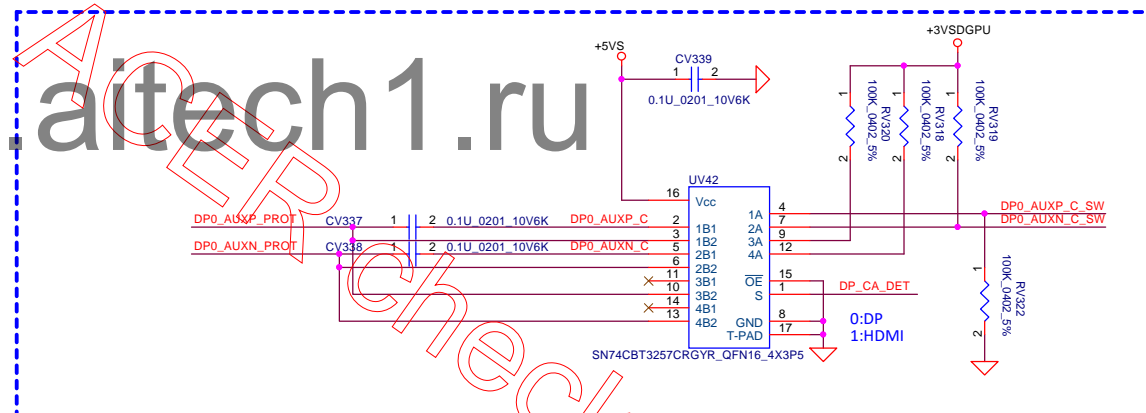
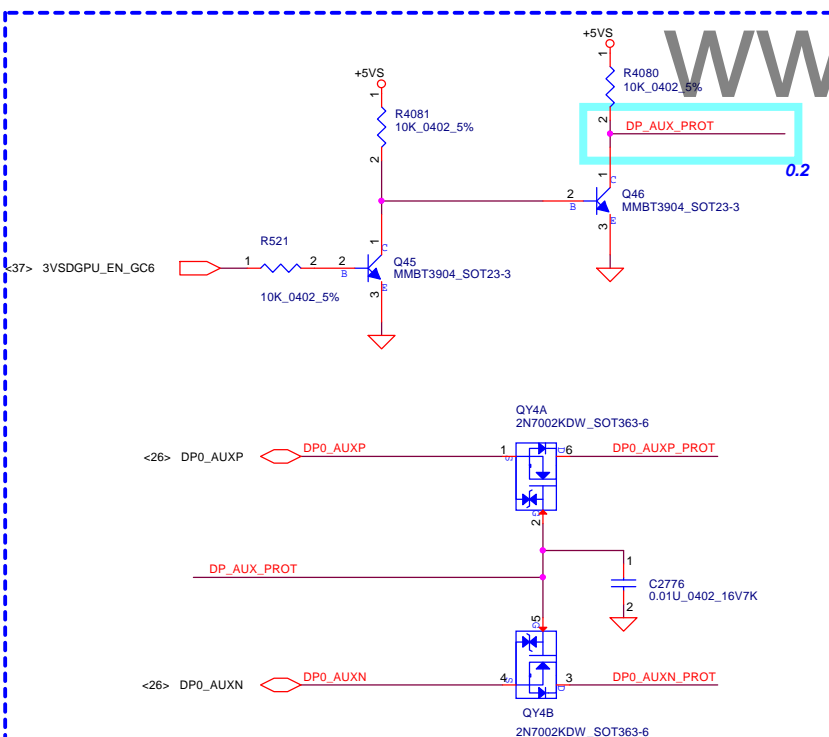
to PCH



### Display Port



## DP++ and isolated circuit



0921 change souce to +3VALW, CTRL to SUSP#

OE#	S	INPUT/OUTPUT A	Function
L	L	B1	A=B1
L	H	B2	A=B2
H	X	Z	NC

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						Size	Document Number				Rev
						Custom	<b>EH78F M/B LA-G161PRO1</b>				0.1
						Date:	Wednesday, January 16, 2019		Sheet	39	of 102



# Raptor

<27> GPU_DP2_P3	CY22	1	2	.1U	0402	16V7K	HDMI_CLKP
<27> GPU_DP2_N3	CY24	1	2	.1U	0402	16V7K	HDMI_CLKN
<27> GPU_DP2_P2	CY16	1	2	.1U	0402	16V7K	HDMI_TX_P0
<27> GPU_DP2_N2	CY17	1	2	.1U	0402	16V7K	HDMI_TX_N0
<27> GPU_DP2_P1	CY18	1	2	.1U	0402	16V7K	HDMI_TX_P1
<27> GPU_DP2_N1	CY19	1	2	.1U	0402	16V7K	HDMI_TX_N1
<27> GPU_DP2_P0	CY20	1	2	.1U	0402	16V7K	HDMI_TX_P2
<27> GPU_DP2_N0	CY21	1	2	.1U	0402	16V7K	HDMI_TX_N2

HDMI\_CLKP RY15 1 2 6.04 0402 1% HDMI\_R\_CLKP

XEMC@ CY26  
3.3P\_0402\_50V8

HDMI\_CLKN RY14 1 2 6.04 0402 1% HDMI\_R\_CLKN

HDMI\_TX\_P0 RY16 1 2 6.04 0402 1% HDMI\_R\_TX\_P0

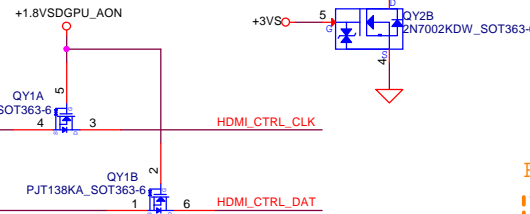
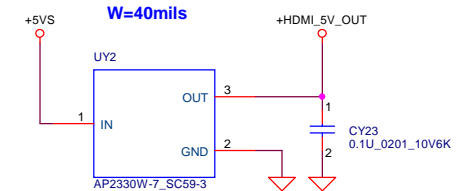
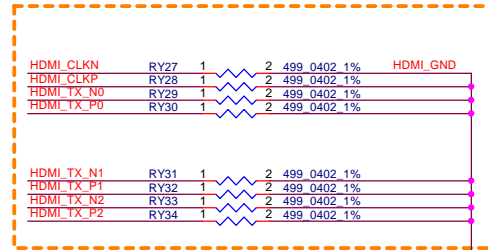
HDMI\_TX\_N0 RY17 1 2 6.04 0402 1% HDMI\_R\_TX\_N0

HDMI\_TX\_P1 RY18 1 2 6.04 0402 1% HDMI\_R\_TX\_P1

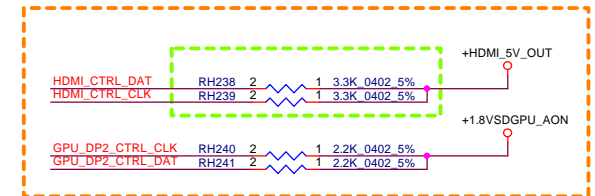
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HDMI\_TX\_P2 RY20 1 2 6.04 0402 1% HDMI\_R\_TX\_P2

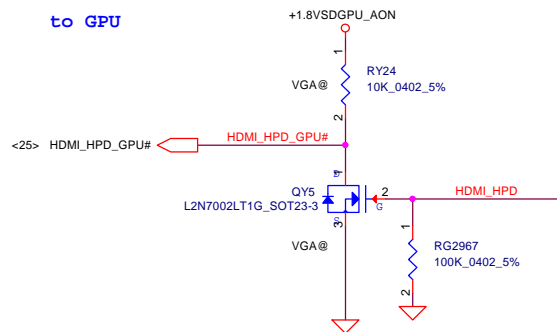
HDMI\_TX\_N2 RY22 1 2 6.04 0402 1% HDMI\_R\_TX\_N2



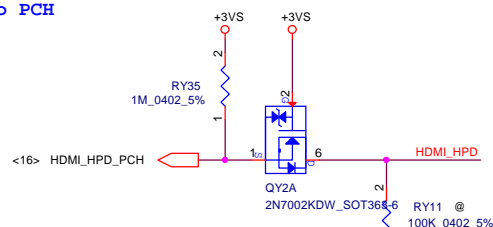
Raptor, follow eagle and 1060 MP 2.2K



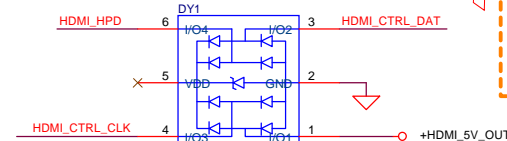
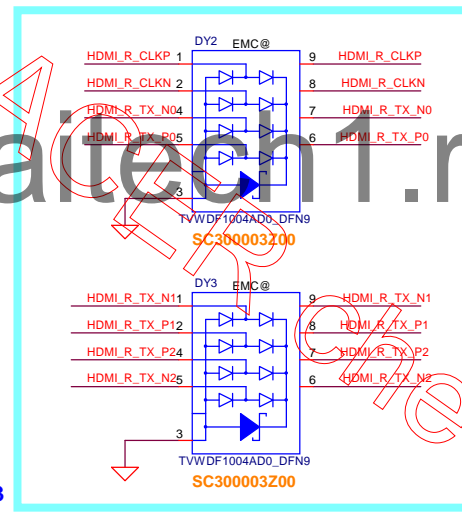
to GPU



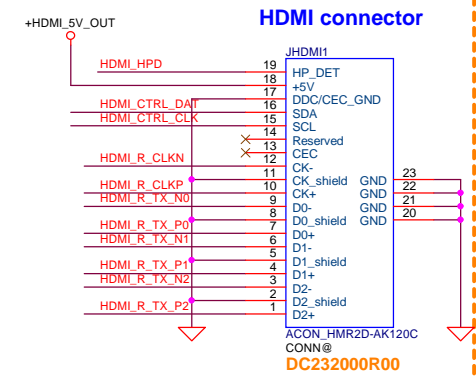
to PCH



change PN follow USB3



P/N: SC300002900, S DIO(BR) AZC199-04S.R7G SOT23-6 ESD



ZZZ2

HDMI ROYALTY  
ROYALTY HDMI W/LOGO+HDCP  
RO0000003HM  
45@

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1012 check Ti if need

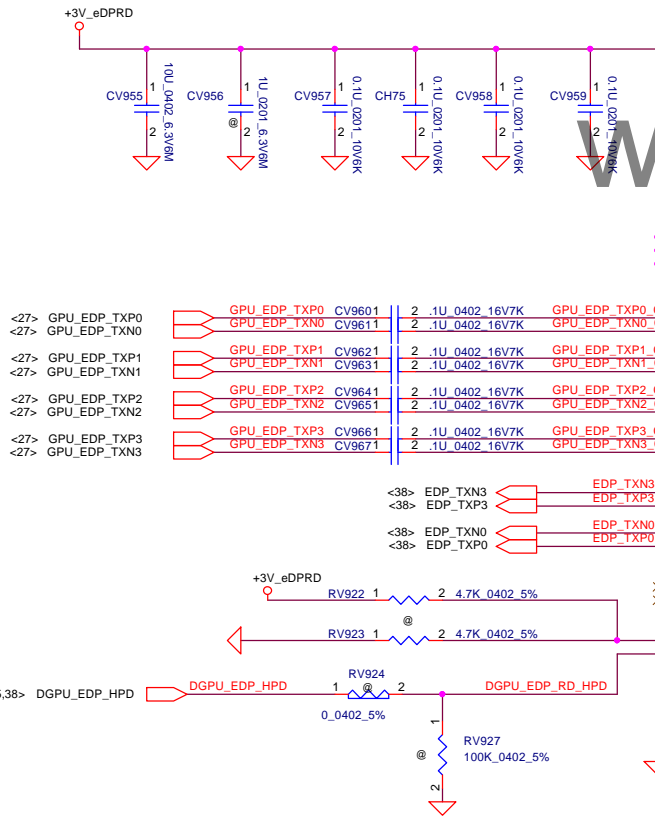
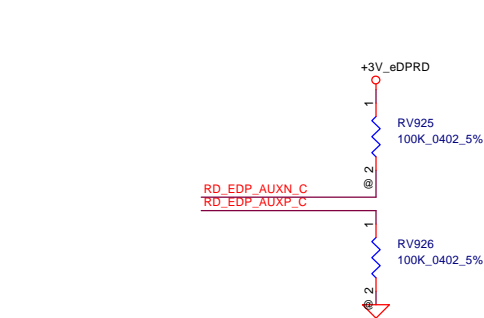
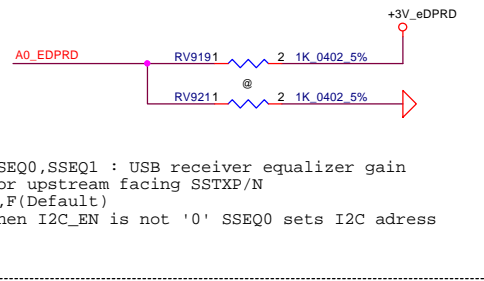
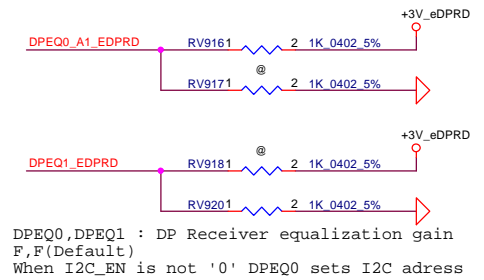
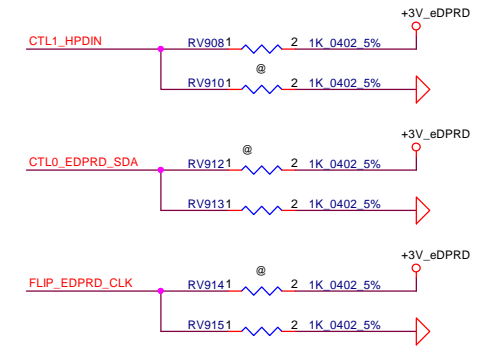
1B

0.2

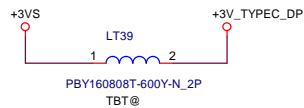
Reserve for 3V power supply

0.2

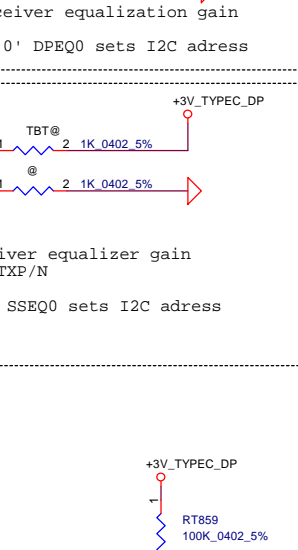
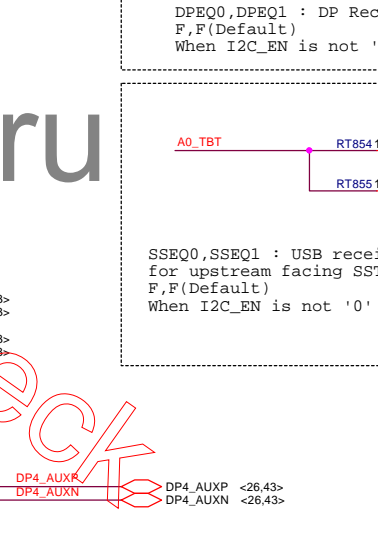
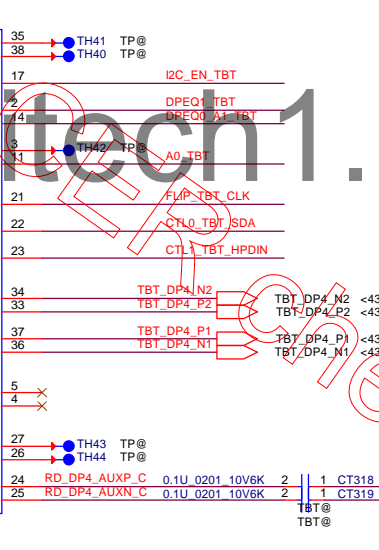
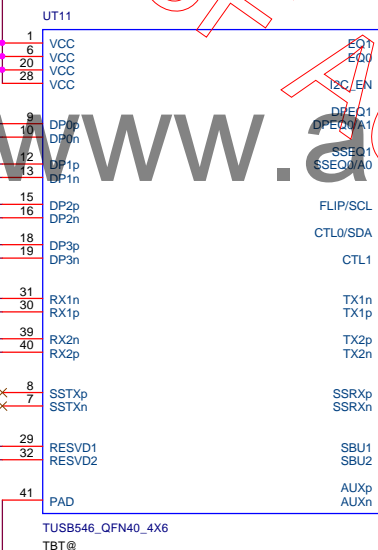
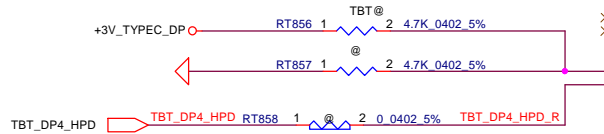
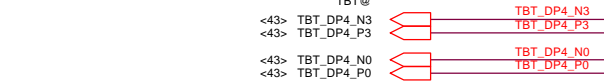
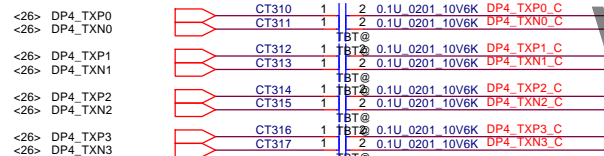
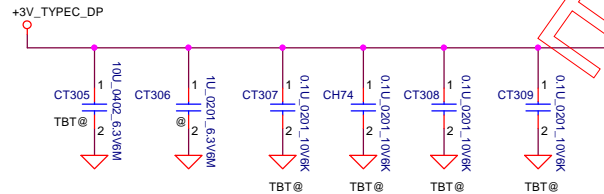
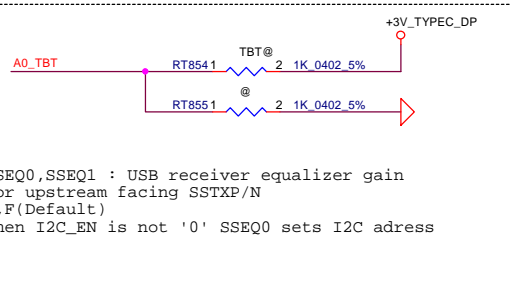
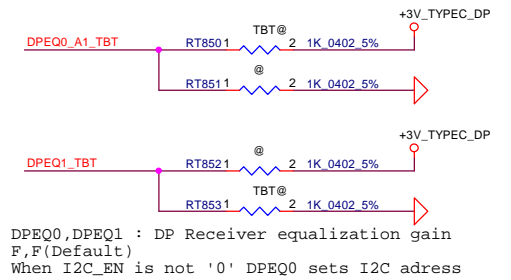
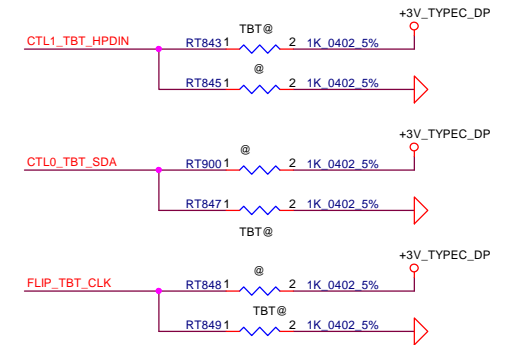
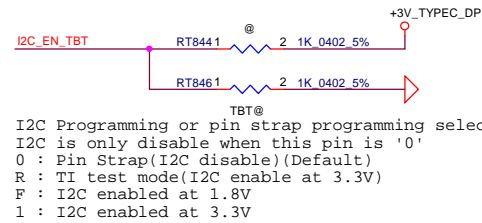
I2C Programming or pin strap programming select.  
I2C is only disable when this pin is '0'  
0 : Pin Strap(I2C disable)(Default)  
R : TI test mode(I2C enable at 3.3V)  
F : I2C enabled at 1.8V  
1 : I2C enabled at 3.3V



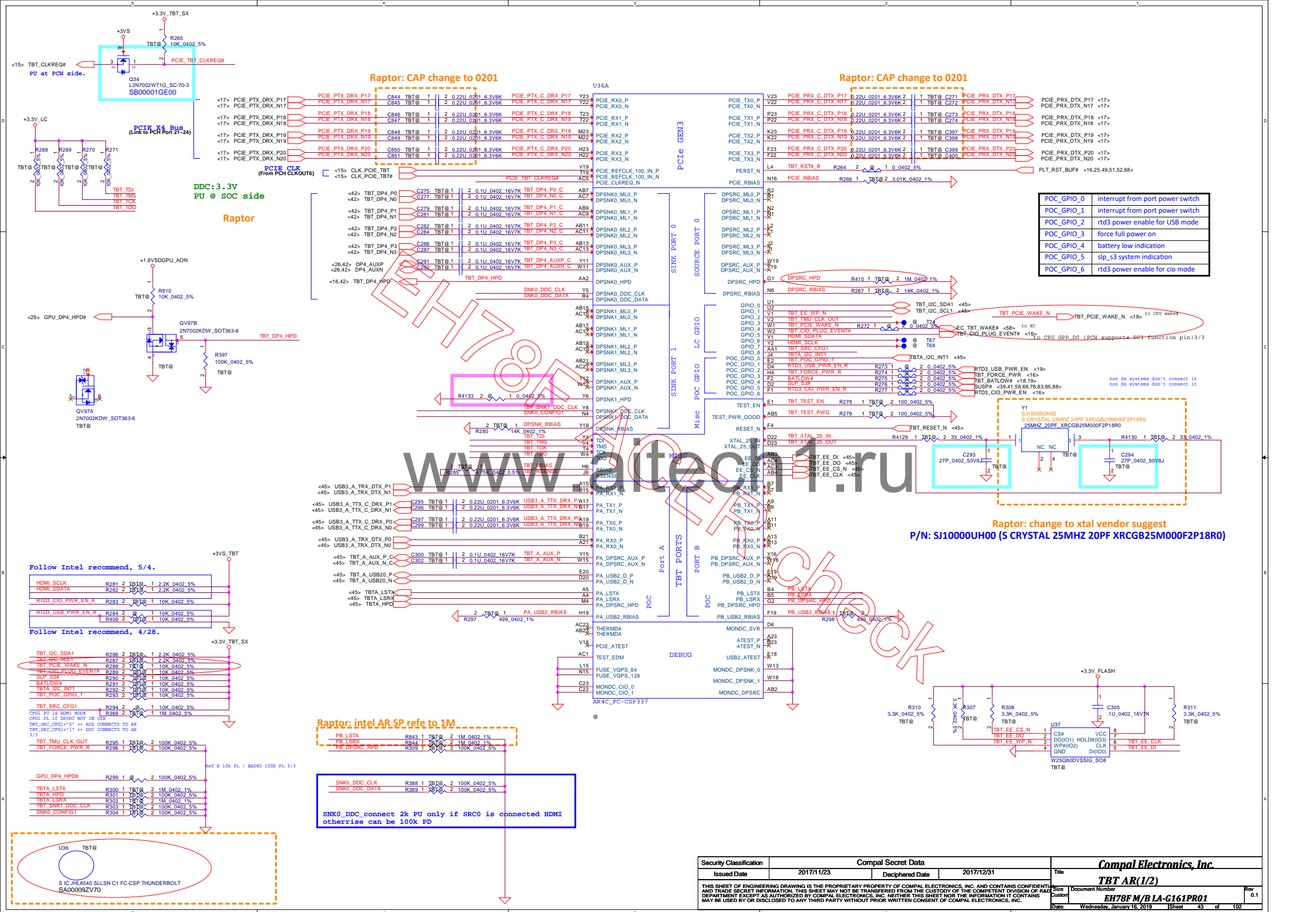
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								Document Number			
								EH78F M/B LA-G161PR01			
								Date			
								Wednesday, January 16, 2019			
								Sheet			
								41 of 102			

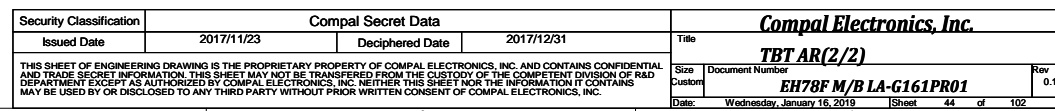
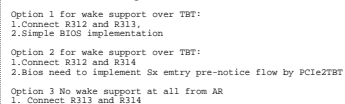


1012 check Ti if need

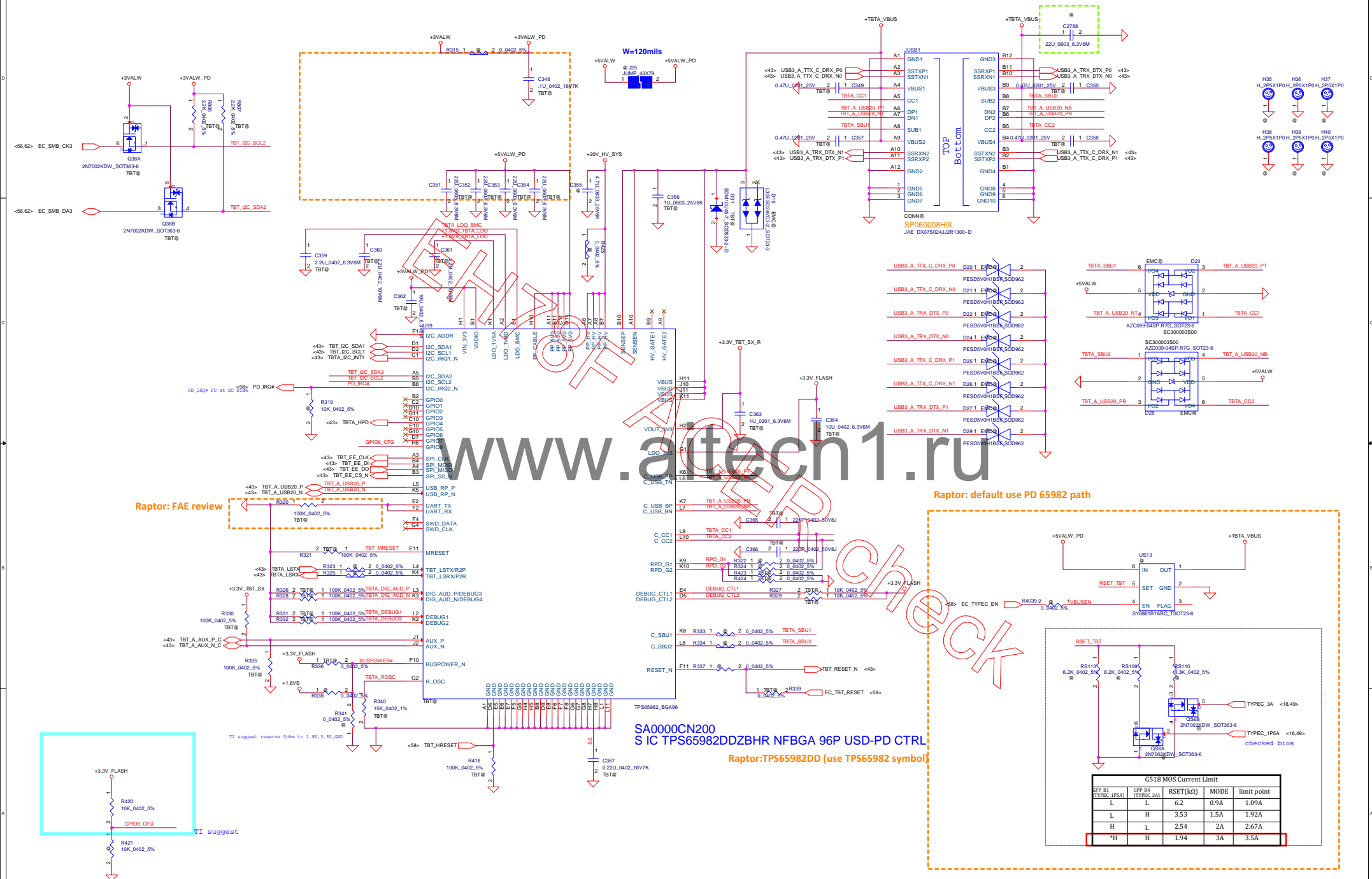


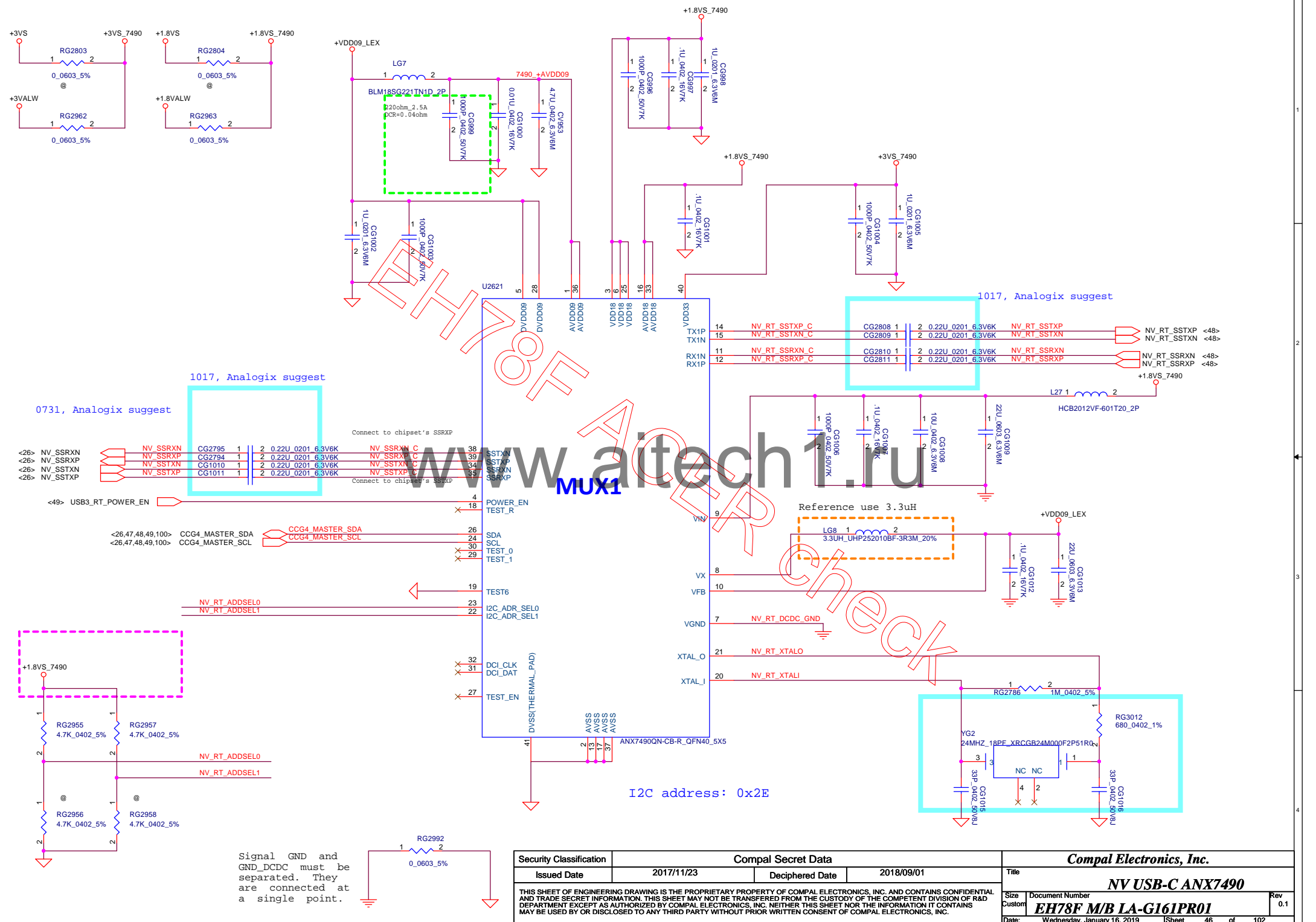
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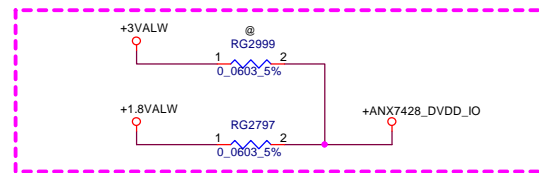
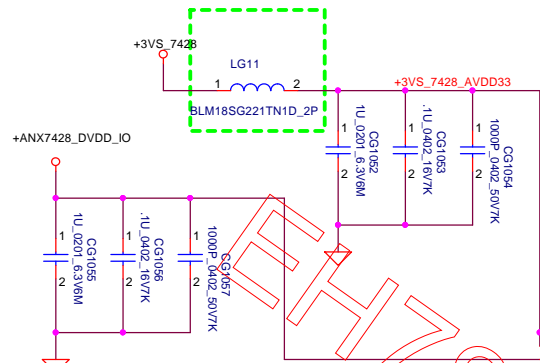
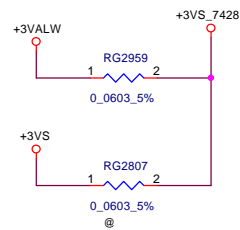






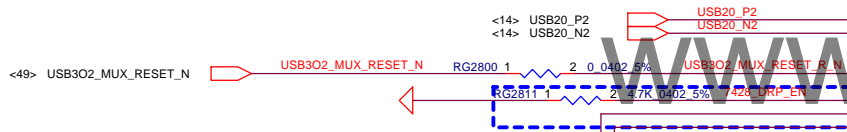
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The DVDD\_IO can be power supplied by 1.8V ~ 3.3V:  
If AP's IO type is 1.8V, select 1.8V power for DVDD\_IO;  
If AP's IO type is 3.3V, select 3.3V power for DVDD\_IO.

0809, follow NV ref design



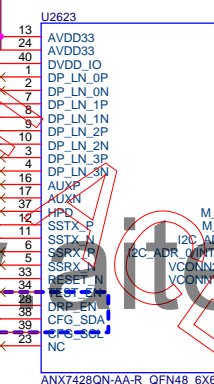
0801, Analogix suggest to pop

RESET\_N pin:  
Controlled by AP or CPU  
Logic 1: Set chip to normal mode.  
Logic 0: Set chip to reset mode.

<26,46,47,49,100> CCG4\_MASTER\_SDA  
<26,46,47,49,100> CCG4\_MASTER\_SCL

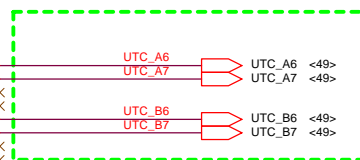
Raptor: I2C PU at CCG4 side

I2C\_ADR\_1 and I2C\_ADR\_0 pin:  
1. The I2C address is determined approximately 500ns after RESET\_N turns from 0 to 1, these two pins' input should be kept at a stable value during this period.  
2. There are internal pull-down resistors on I2C\_ADR\_0 and I2C\_ADR\_1 pins.  
3. If external pull-up resistor is not populated, the I2C\_ADR\_0 or I2C\_ADR\_1 is logic 0.  
4. If external pull-up is populated, the I2C\_ADR\_0 or I2C\_ADR\_1 is logic 1.

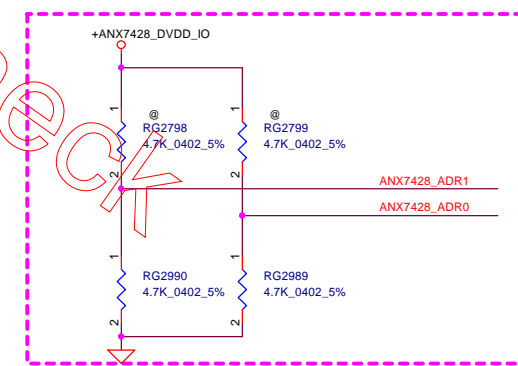
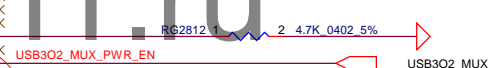
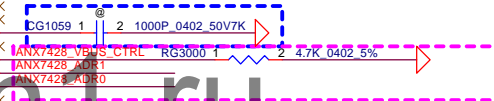


SA000094H10

I2C address: 0x80

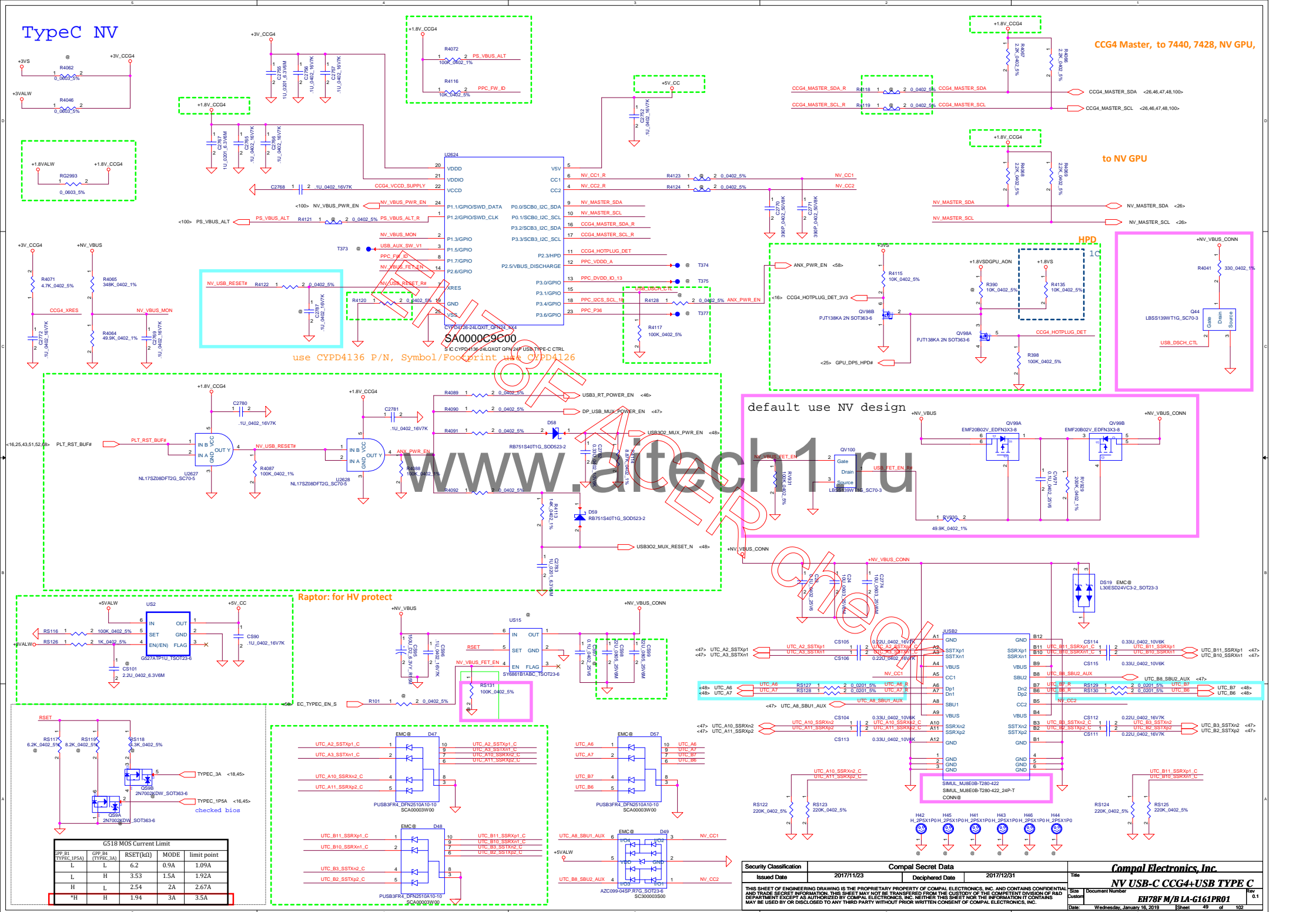


0731, Analogix suggest to NC



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## TypeC NV



G518 MOS Current Limit				
GPP_B1 (TYPEC_1P5A)	GPP_B4 (TYPEC_3A)	RSET(kΩ)	MODE	limit point
L	L	6.2	0.9A	1.09A
L	H	3.53	1.5A	1.92A
H	L	2.54	2A	2.67A
*H	H	1.94	3A	3.5A



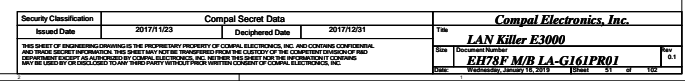
EH78F M/B LA-G161PR01

**Reserve Page**

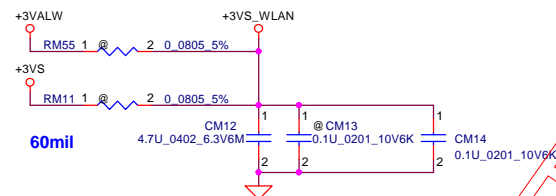
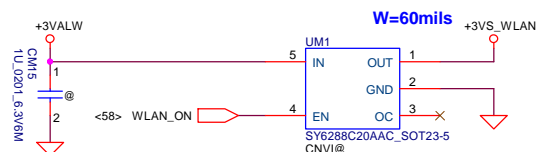
www.aitech1.ru

check

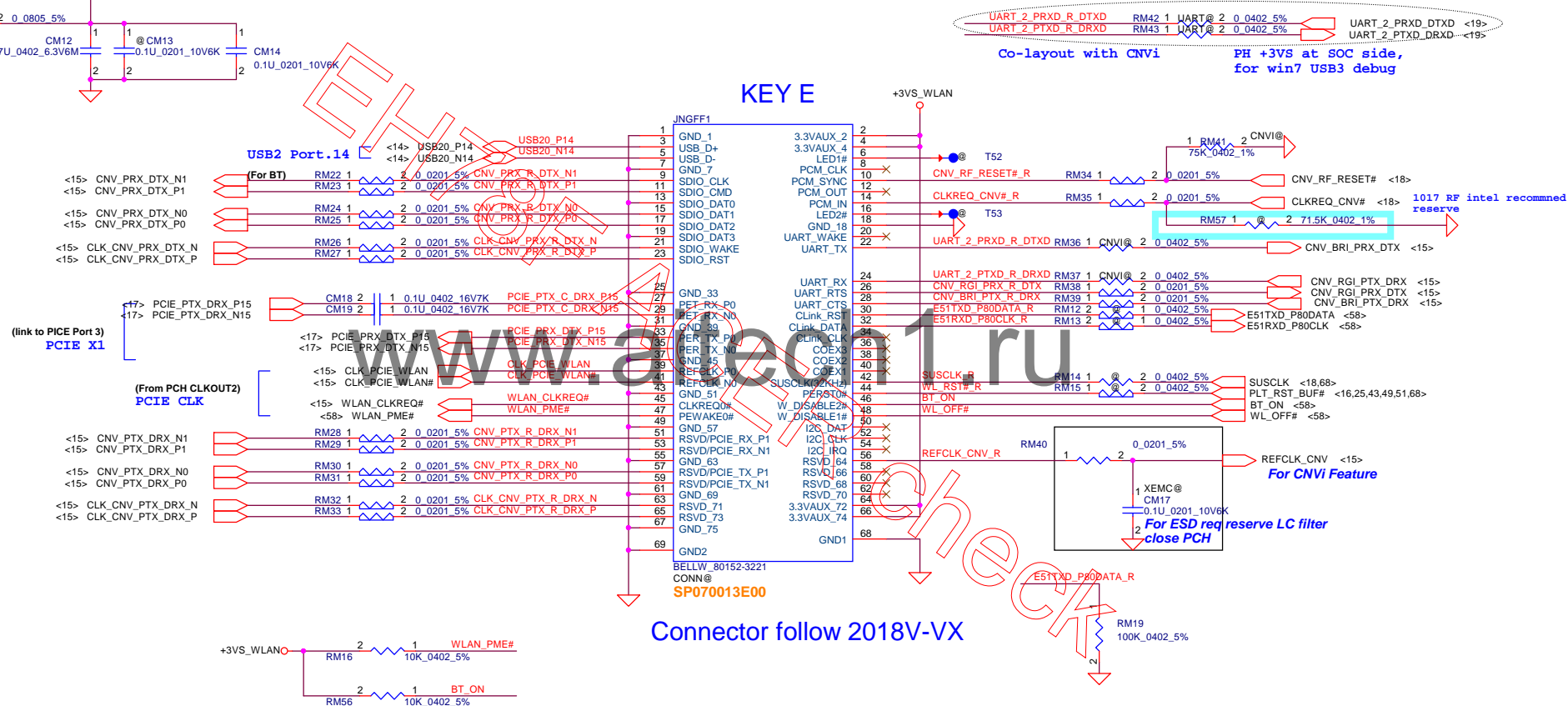
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# Wireless LAN



## NGFF WL+BT (KEY E)



Connector follow 2018V-VX

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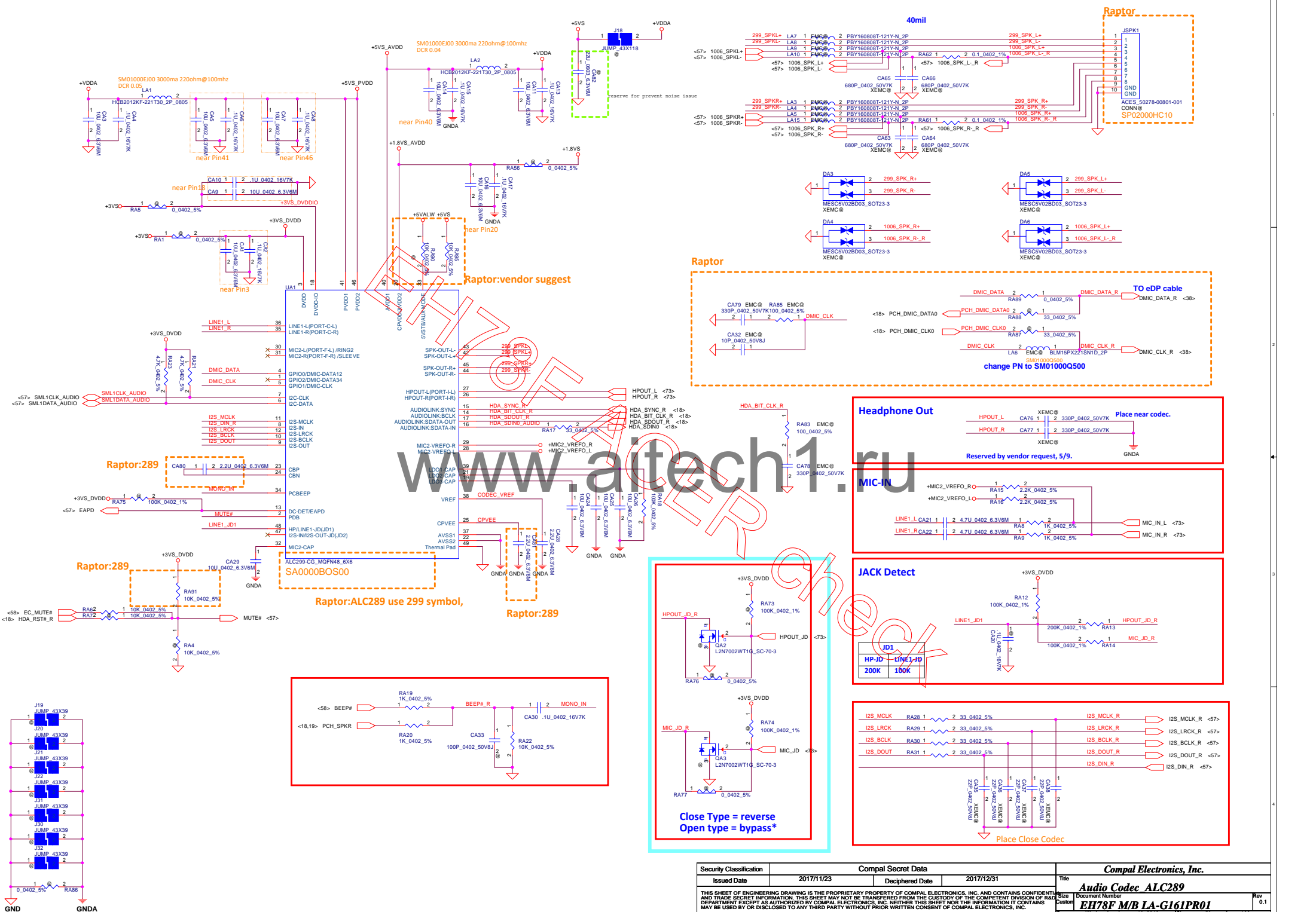
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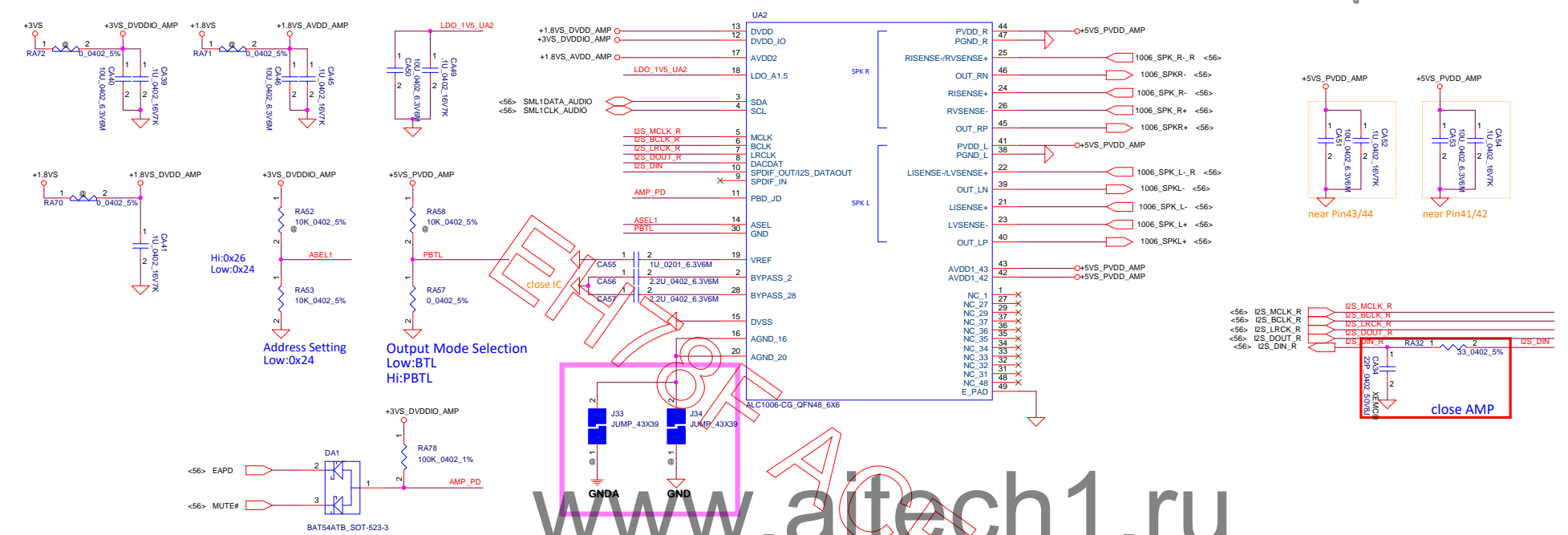
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For SPK Conn.



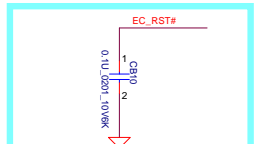
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Raptor:Realtek update the design connect to GND, default J34

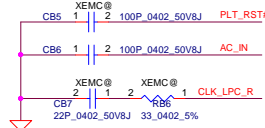
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Issued Date				2017/11/23				Title			
Deciphered Date				2017/12/31				Audio Amplifier ALC1006			
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				Customer				EH78F M/B LA-G161P01			
				Date				Wednesday, January 16, 2019			
				Sheet				57 of 102			



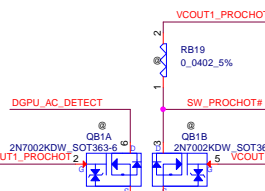
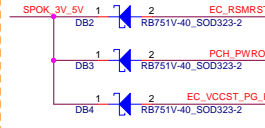
Prevent EC CLK test mode issue



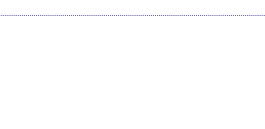
For turn off internal LPC module of KB9032



Raptor: 3V/5V combine solution



for marco key 3810



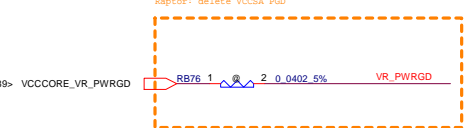
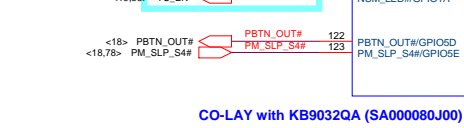
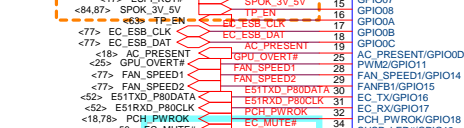
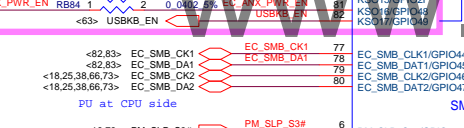
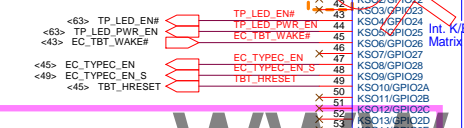
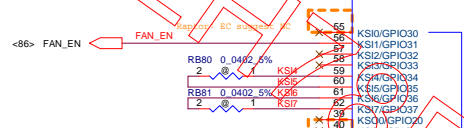
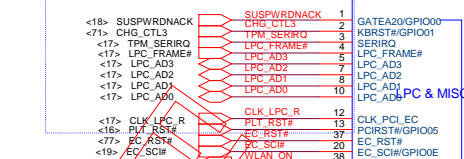
Raptor: delete VCCSA PBD



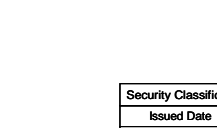
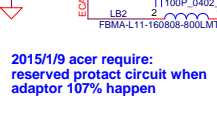
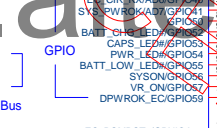
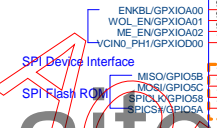
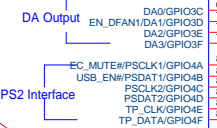
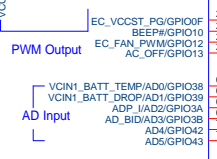
For Power consumption Measurement



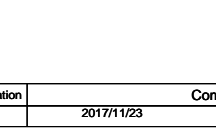
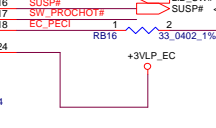
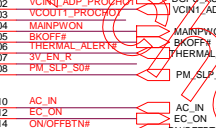
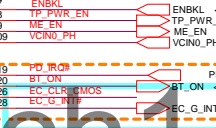
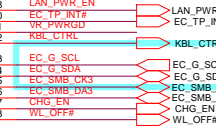
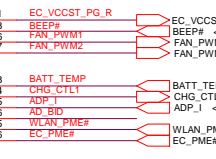
ESPI Bus Pin : 1-5,7,8,10,12,14  
LPC Bus Pin : 3-5,7,8,10,12,13



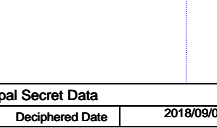
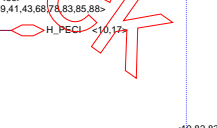
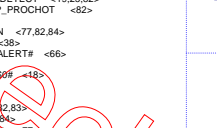
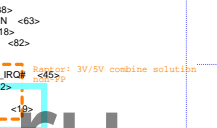
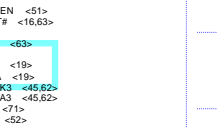
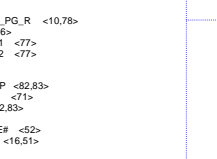
check VR\_PWRGD IS AND BY CORE\_PWRGD & SA\_PWRGD



2015/1/9 acer require: reserved protect circuit when adaptor 107% happen

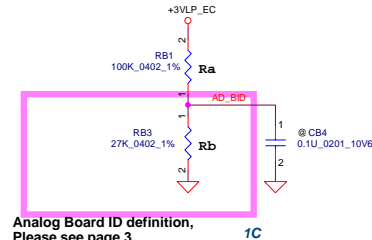


2015/1/9 acer require: reserved protect circuit when adaptor 107% happen



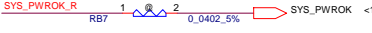
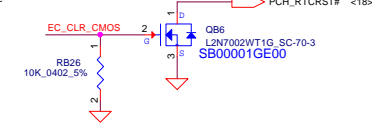
2015/1/9 acer require: reserved protect circuit when adaptor 107% happen

Board ID

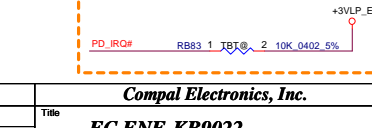
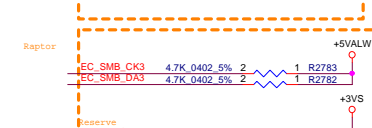
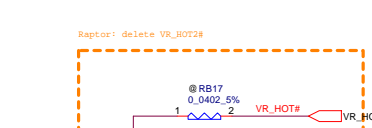
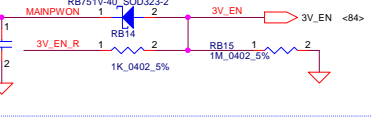


Analog Board ID definition, Please see page 3.

near SOC



For Thermal Portect Shutdown



Raptor: delete VR\_HOT#

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				Sheet 59 of 102	



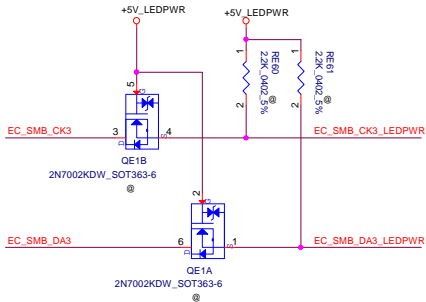
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				Date: Wednesday, January 16, 2019	Rev 0.1
				Sheet 60 of 102	

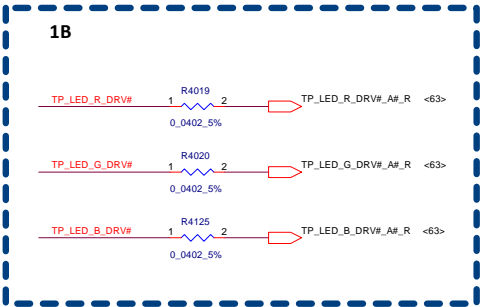


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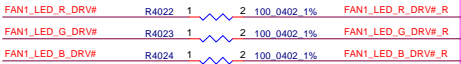
Reserve, default bypass



T/P

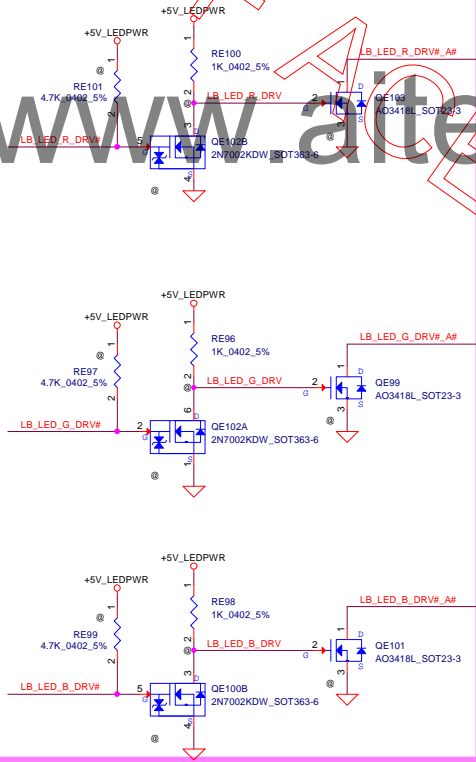


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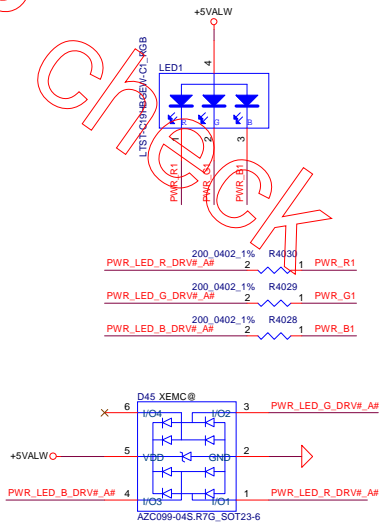
QE100A  
2N7002KDW\_SOT363-6

LED/B

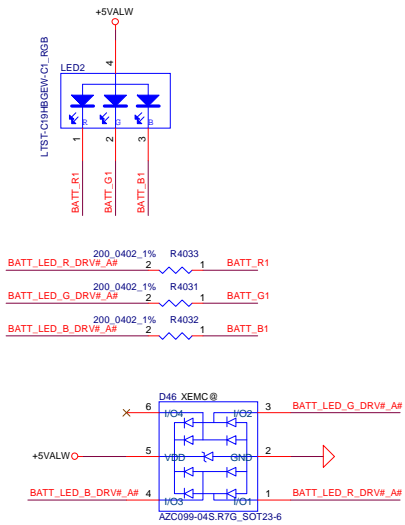


PWRBTN LED

PWR LED

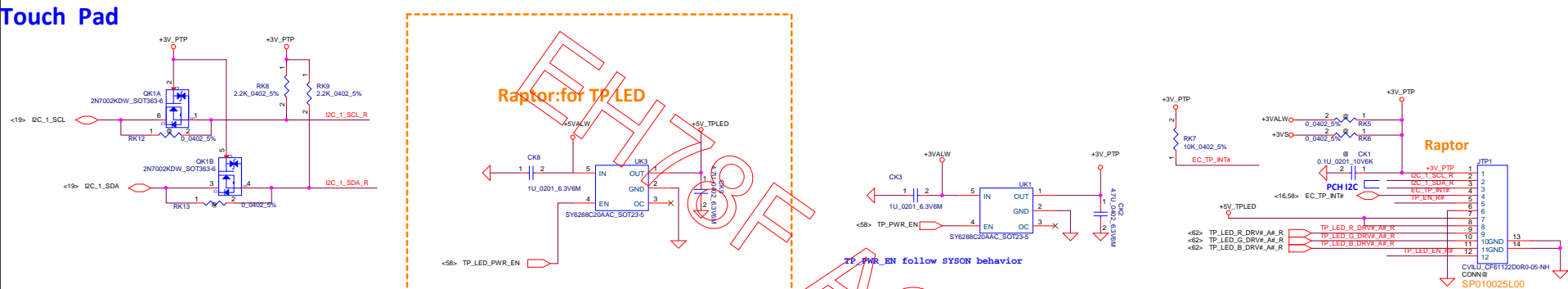


BATT LED



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## Touch Pad



Raptor:waiting more spec for check



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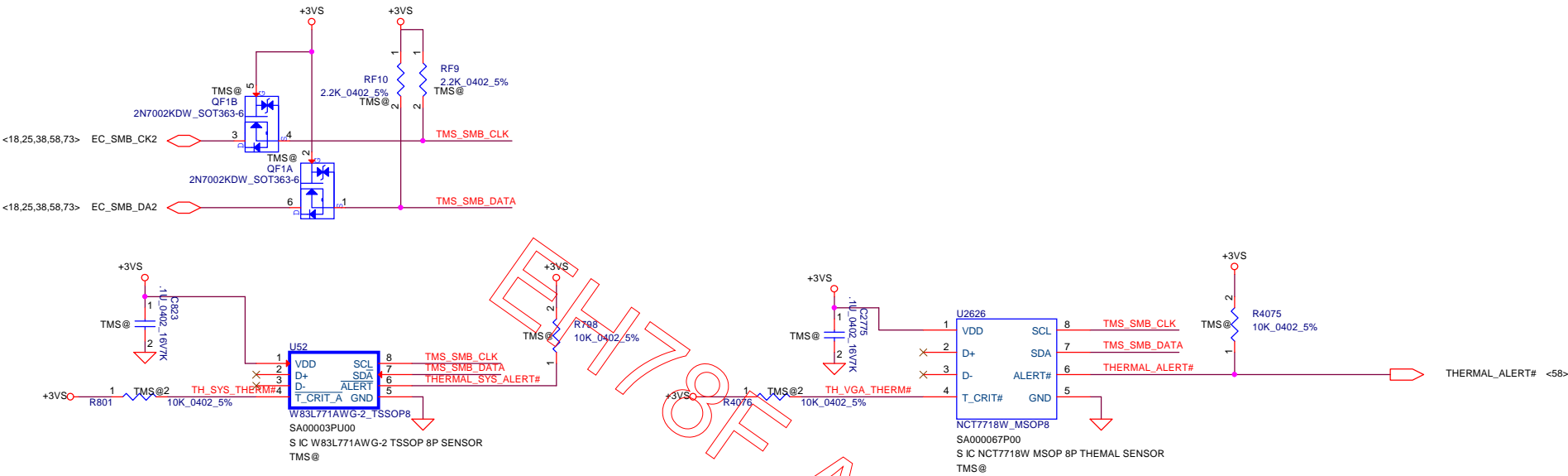
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Issued Date	2017/11/23	Deciphered Date	2018/09/01	Title	Reserve Page
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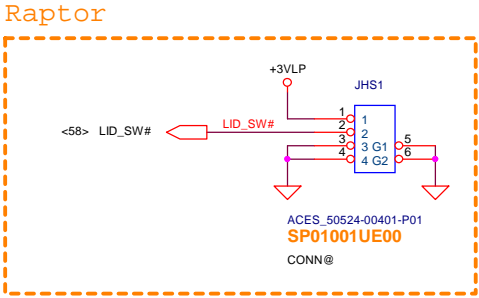
THERMAL SENSOR



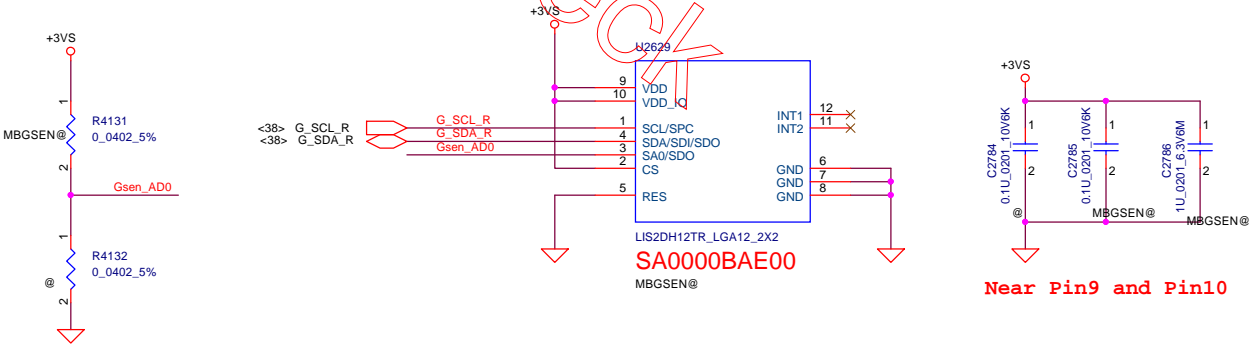
Part Number      SMBUS ADDRESS  
NCT7718W            1001\_1000b  
W83L771AWG-2      1001\_1010b

www.aitech1.ru

To Hall sensor/B



M/B Gsensor

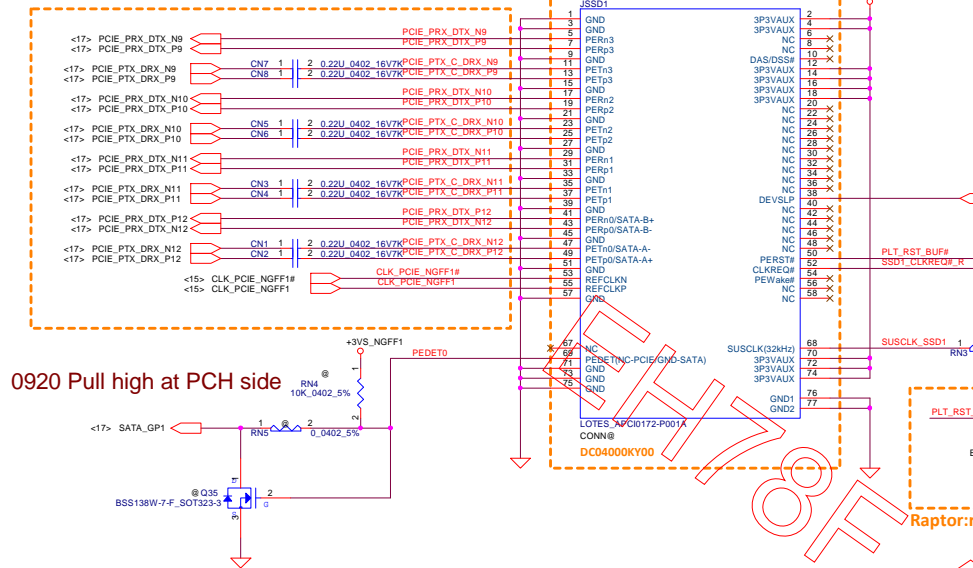


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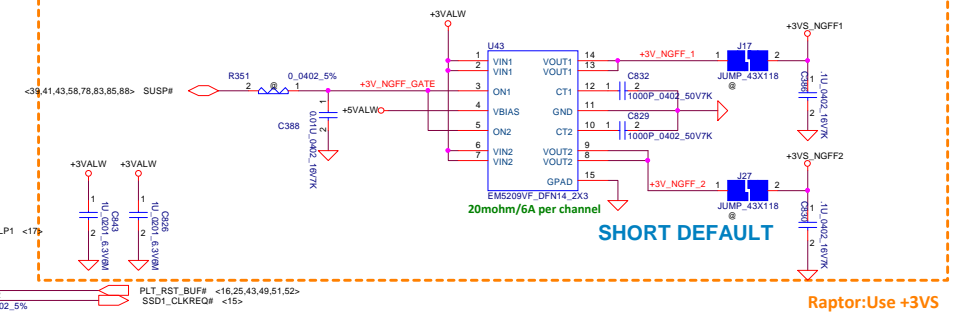
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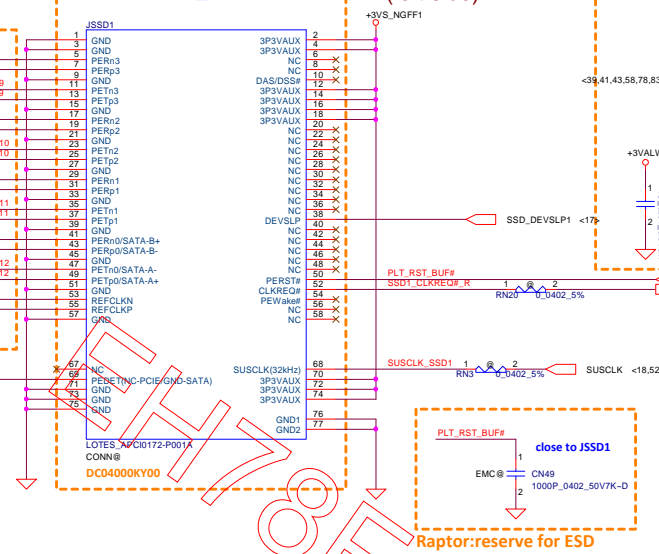
# Raptor:LANE REVERSAL for SATA/PCIE Combo Lanes



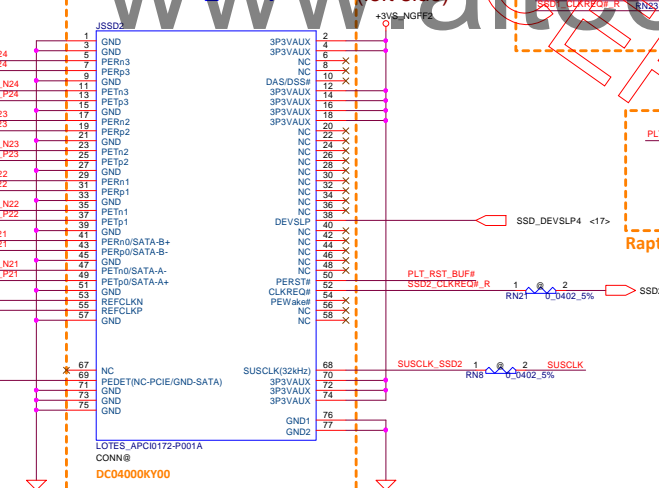
## +3VS\_NGFF PWR



## SSD NGFF Slot\_1 Key M



## SSD NGFF Slot\_2 Key M



PEDET	Module Type
0	SATA
1	PCIE

PEDET	Module Type
0	SATA
1	PCIE

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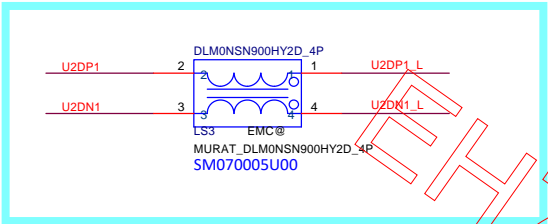
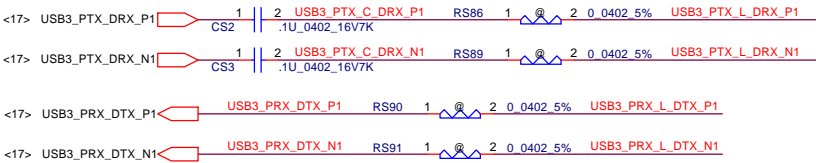
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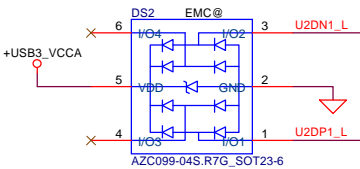
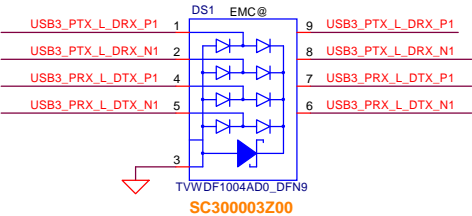
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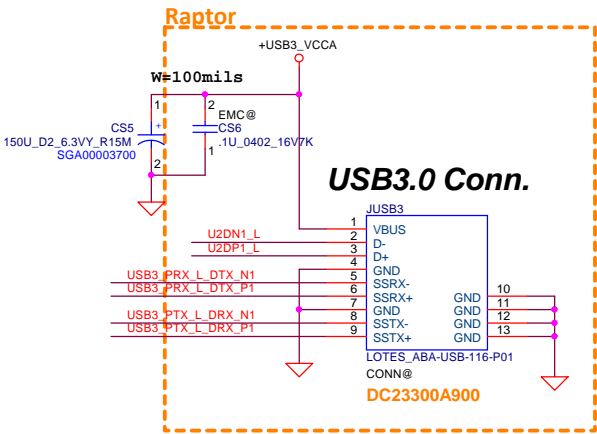
USB3.0 /2.0 CMC



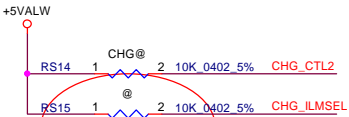
correct footprint to MURAT\_DLM0NSN900HY2D\_4P



Charger Port



USB Host Charger



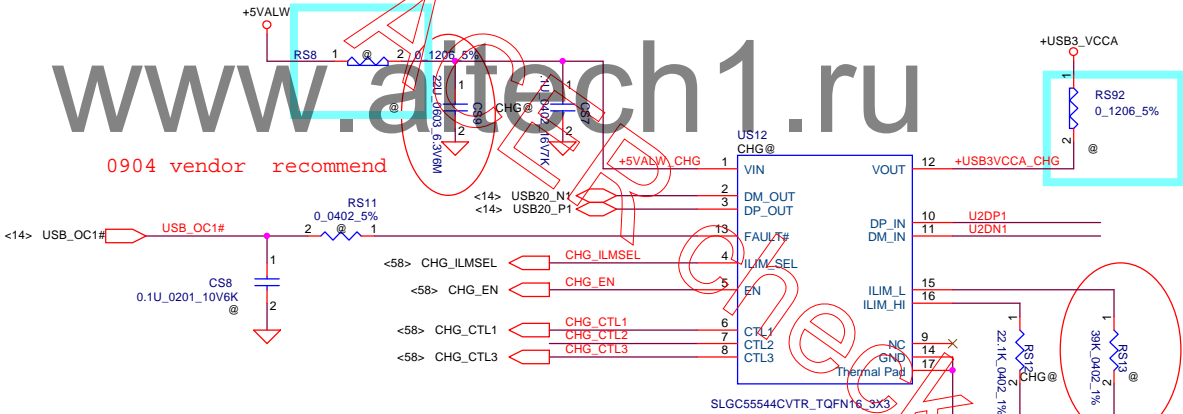
0911 Rerserve PU, vendor suggest to EC control if future need support SDP2

USB Host Charger Truth Table

CHG_EN	CTL1	CTL2	CTL3	ILIM_SEL	MODE	Current Limit Setting	Note
0	0	1	0	1	SDP1-OFF	ILIM_H	Port power off
1	0	1	0	1	SDP1	ILIM_H	Data Lines Connected
1	0	1	1	1	DCP Auto	ILIM_H	Data Lines Disconnected
1	1	1	1	1	CDP	ILIM_H	Data Lines Connected

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0904 vendor recommend



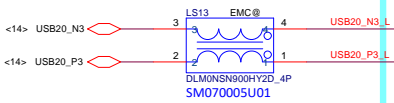
0831 Reserve ILIM\_L R as vendor recommend

ILM R vaule  
Ios(mA)=50250/R(Kohm)  
ILIM\_Hi=2273mA  
ILIM\_L=1288mA(reserve)

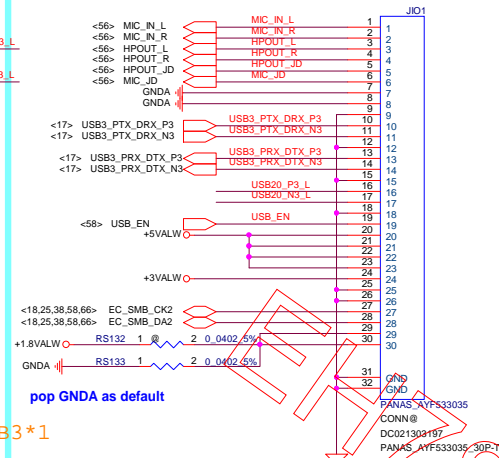
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				Date: Wednesday, January 16, 2019	Rev 0.1
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## USB\_Audio/B



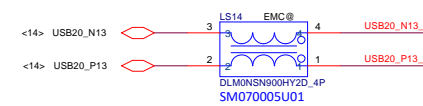
## Raptor



pop GND as default

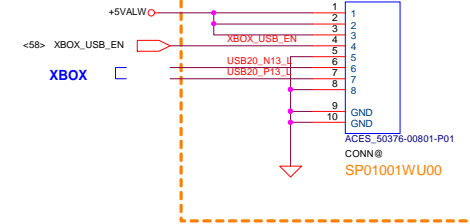
Raptor: MIC+Headphone+USB3\*1

## XBOX/B



XBOX

## Raptor



Raptor: 1\*USB2.0

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				Sheet 75 of 102	

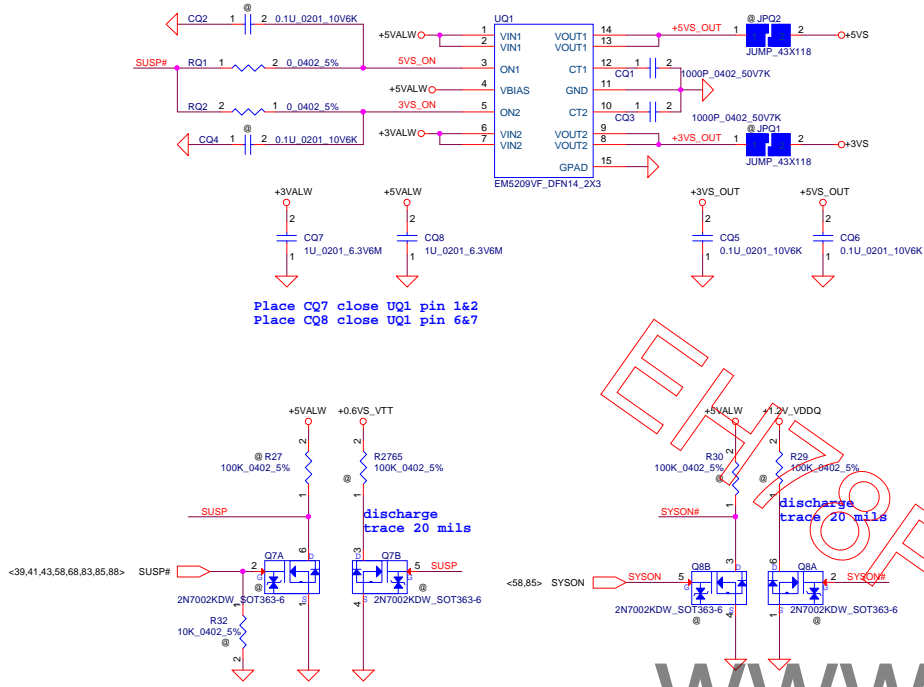


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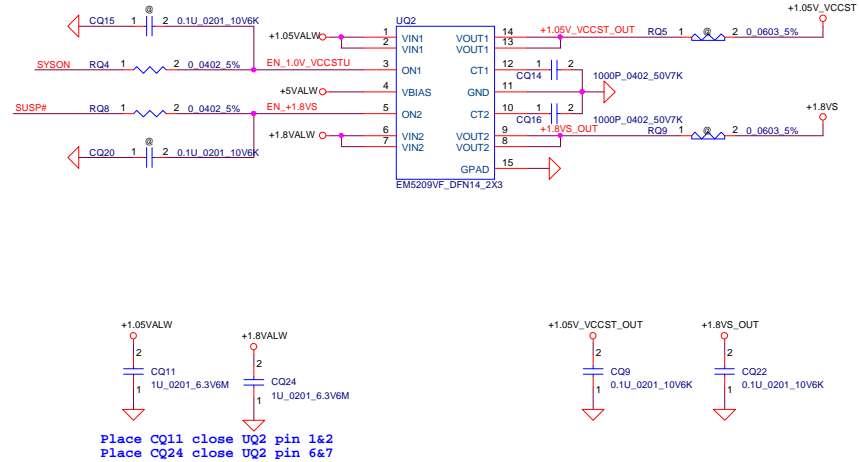
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		Document Number		EH78F M/B LA-G161PR01	
		Date: Wednesday, January 16, 2019		Sheet	76 of 102



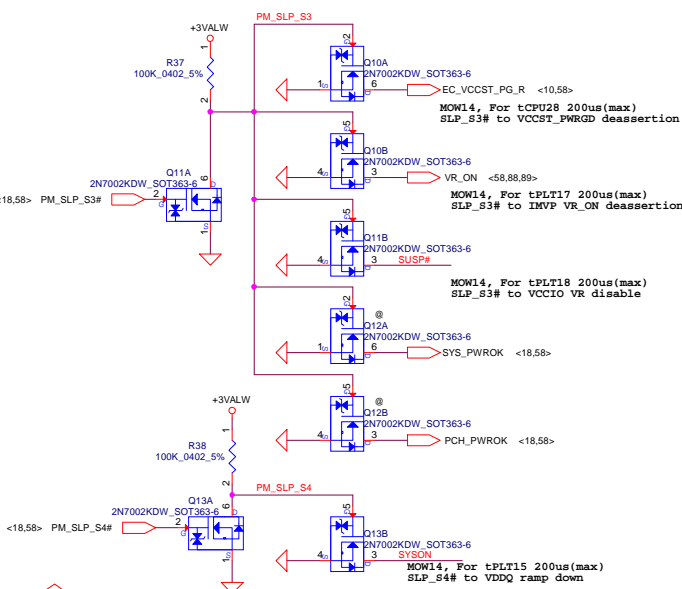
System DC interface



+1.05VALW TO +1.05V\_VCCST /+1.8VALW TO +1.8VS

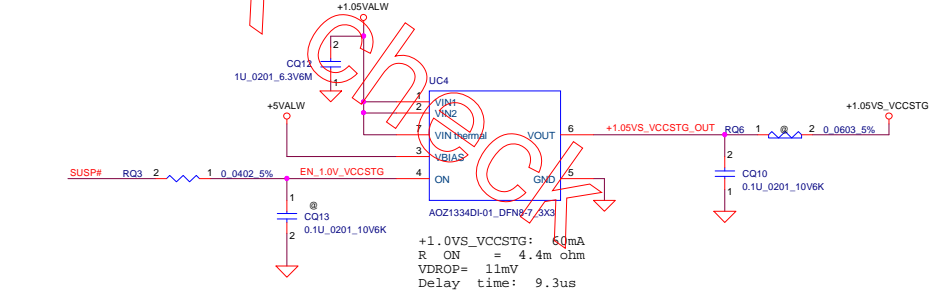


For Power ON/Off Sequence



P/N: SB00000E000 footprint use SB00000ZU00

+1.05VALW TO +1.05VS\_VCCSTG



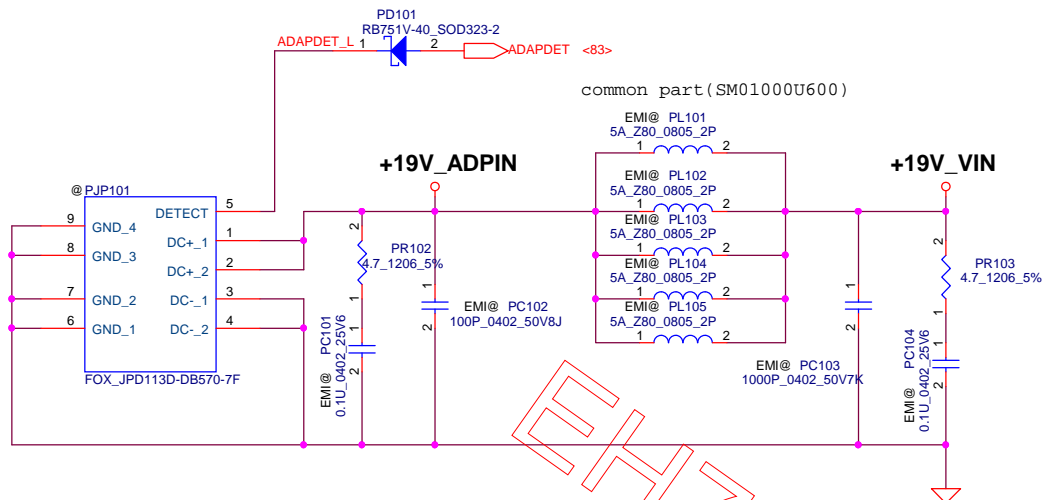
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Issued Date	2017/11/23	Deciphered Date	2018/09/01	Title	DC INTERFACE
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				Date: Wednesday, January 16, 2019	Rev 0.1
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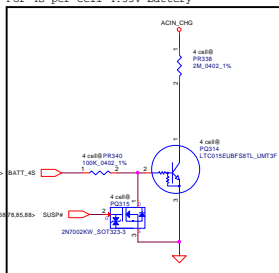
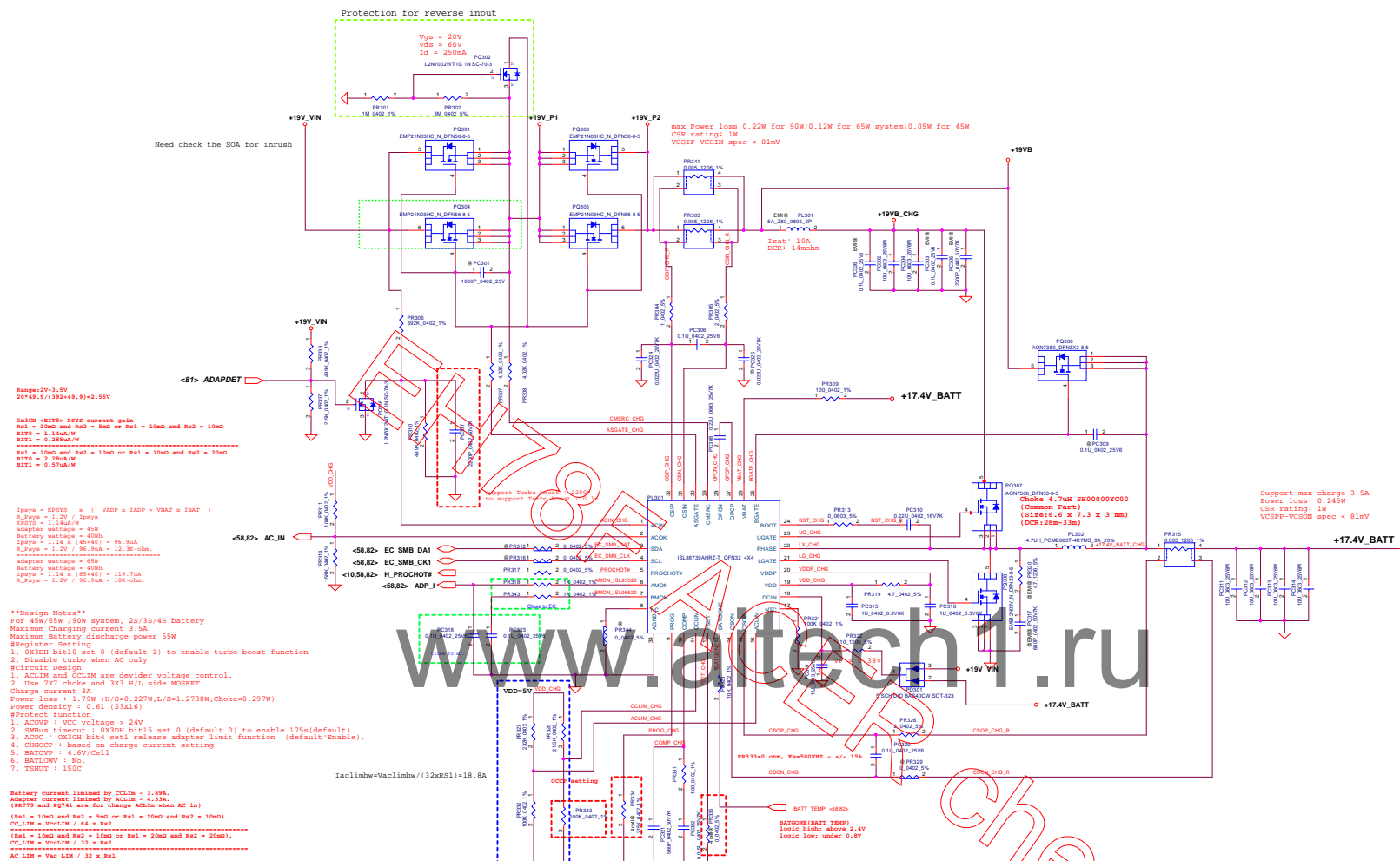


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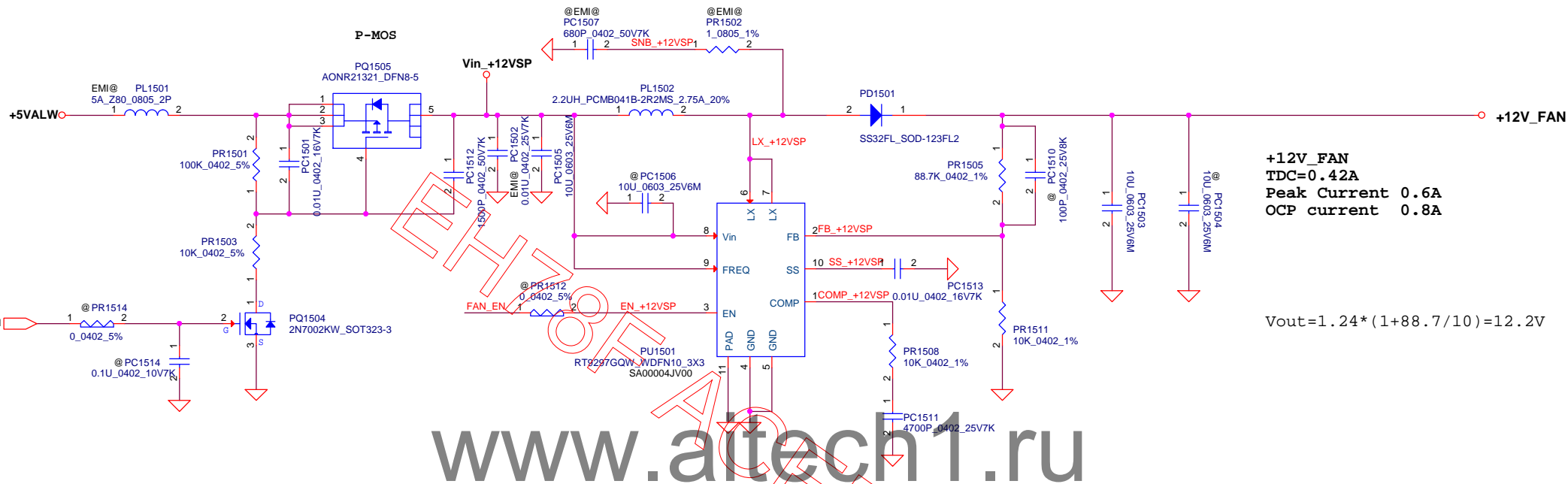








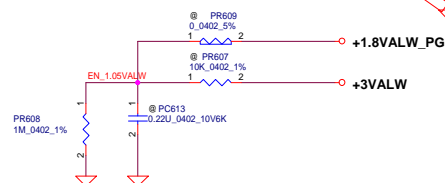
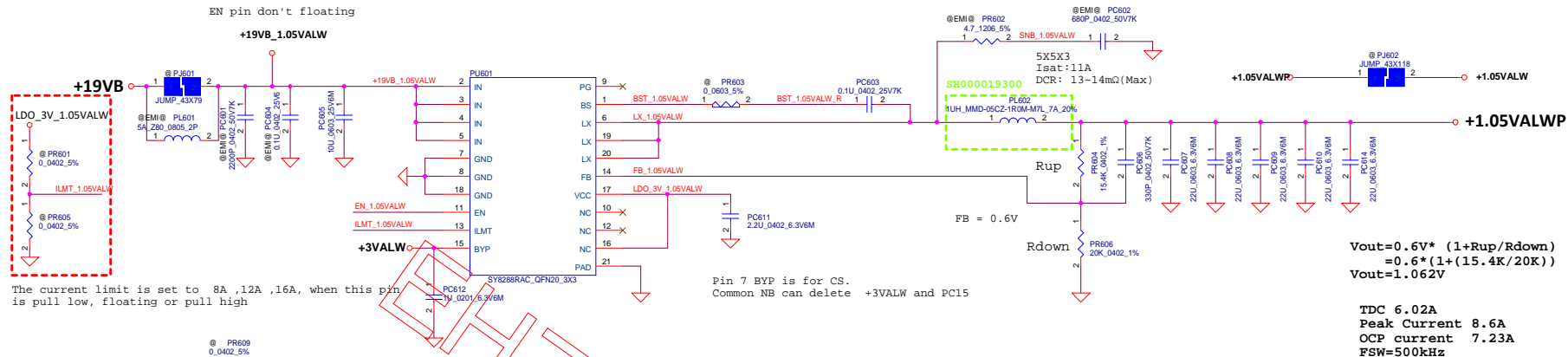
SH00000B600  
4X4X1.2  
Isat: 3.5A  
DCR: 83.5mΩ (Max)



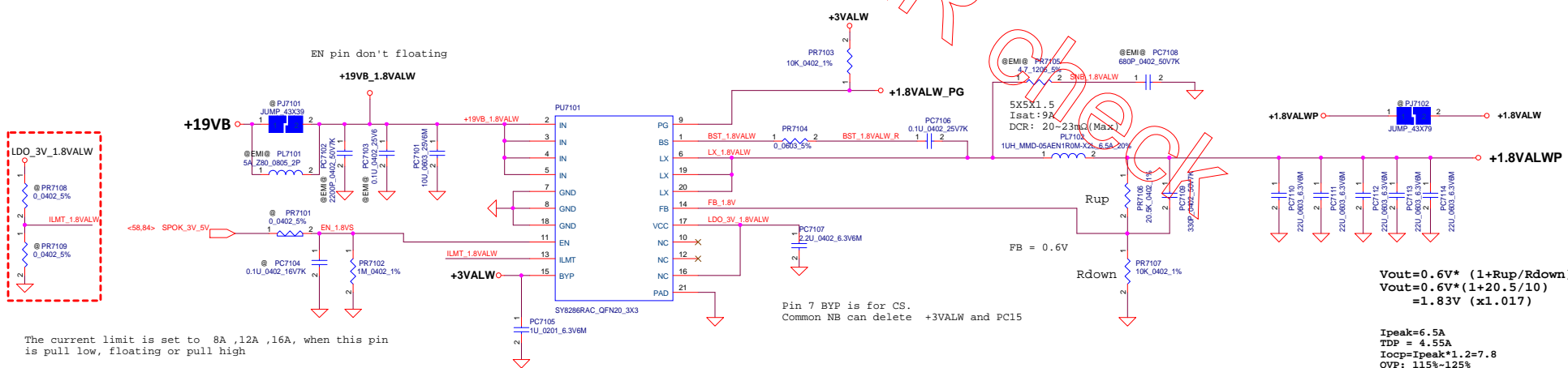
+12V\_FAN  
TDC=0.42A  
Peak Current 0.6A  
OCP current 0.8A

$$V_{out} = 1.24 * (1 + 88.7/10) = 12.2V$$

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				Date:	Wednesday, January 16, 2019
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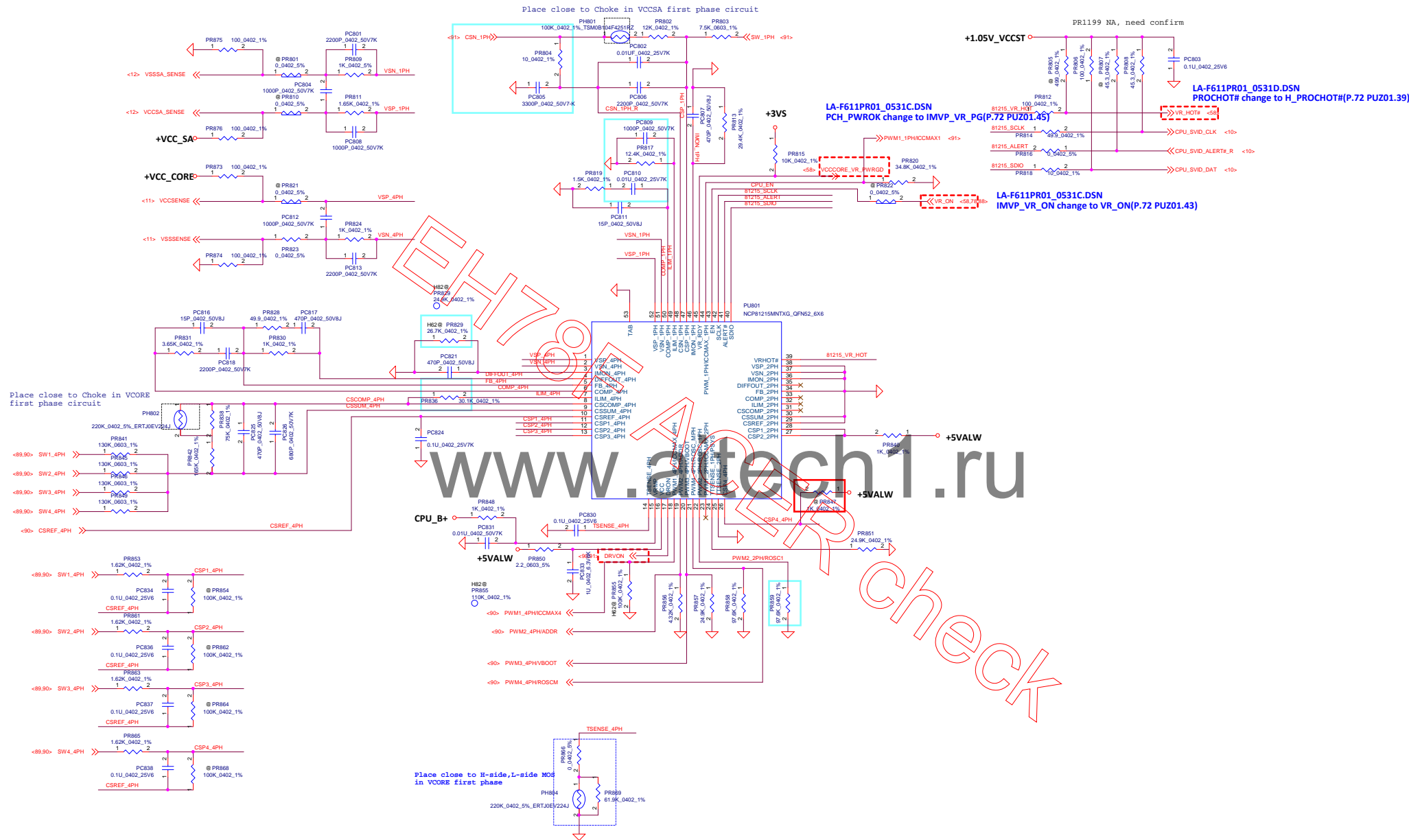
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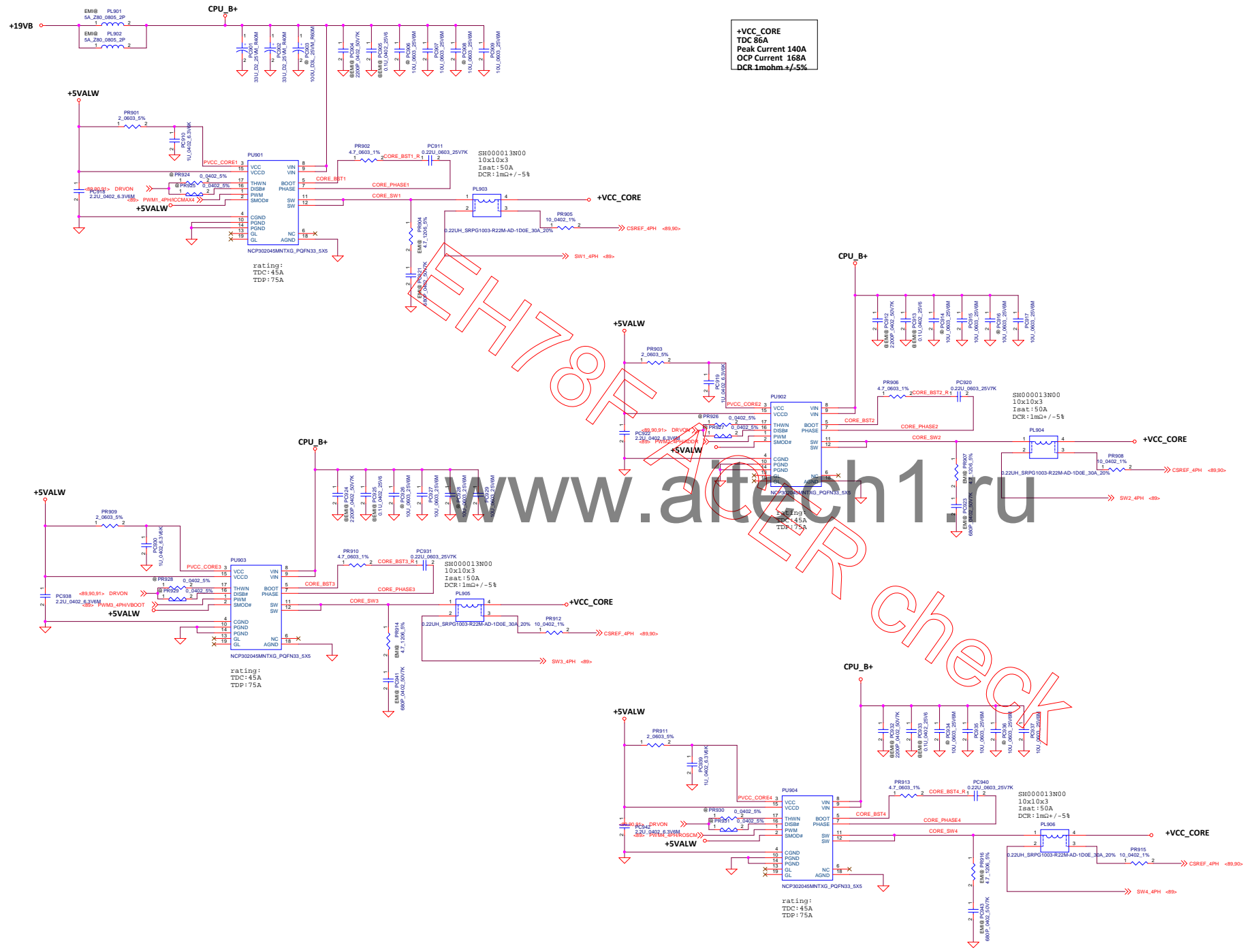
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				Size	Rev
				Document Number	0.1
				CIPRG LA-E051P	
				Date	Wednesday, January 16, 2019
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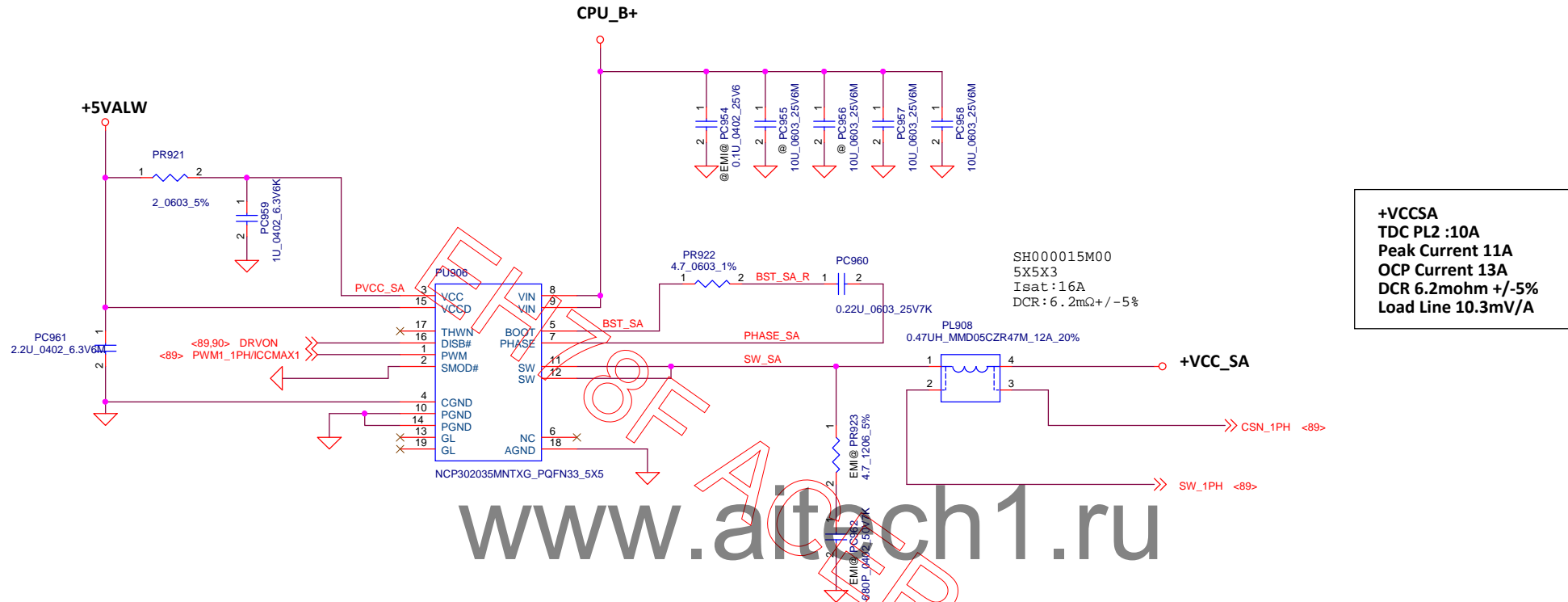




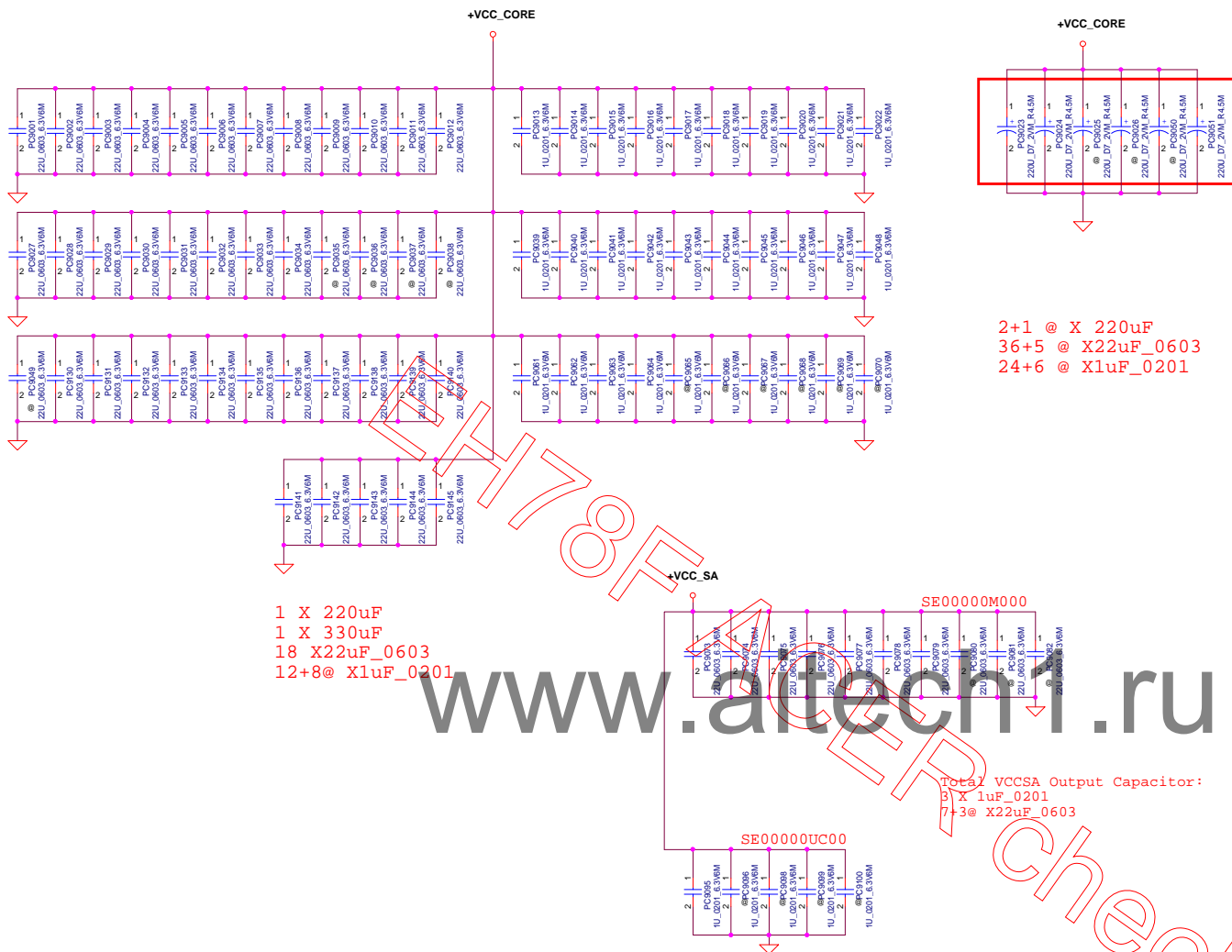
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				Custom	CPU IC SKL H 42
				Date	Wednesday, January 16, 2019
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				Rev	0.1



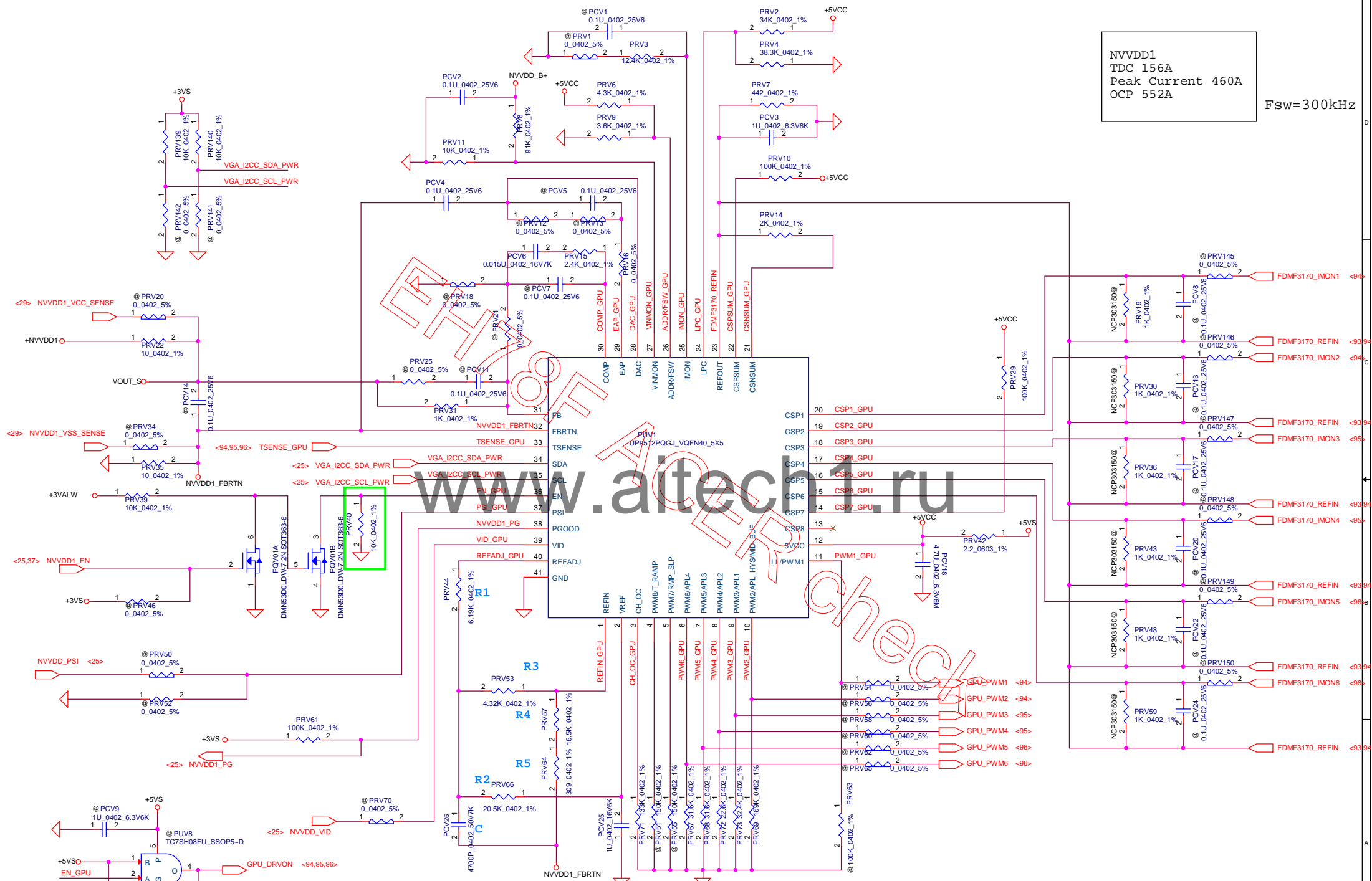
Main Func = VCCGT/+VCCSA



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				CIPRG LA-E051P	
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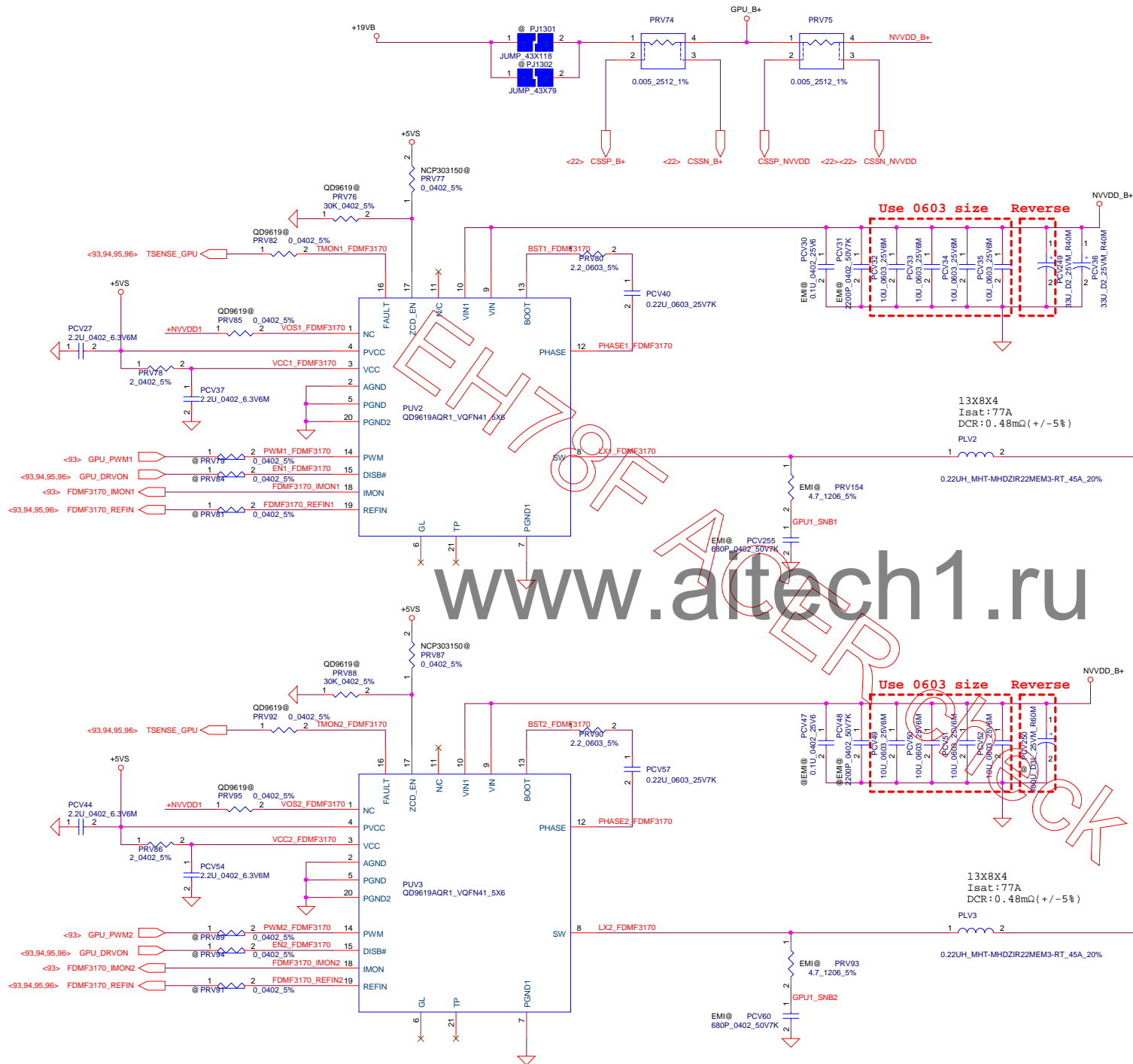
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PWNVID 的RC BOM  
请根据GPU's config 设定

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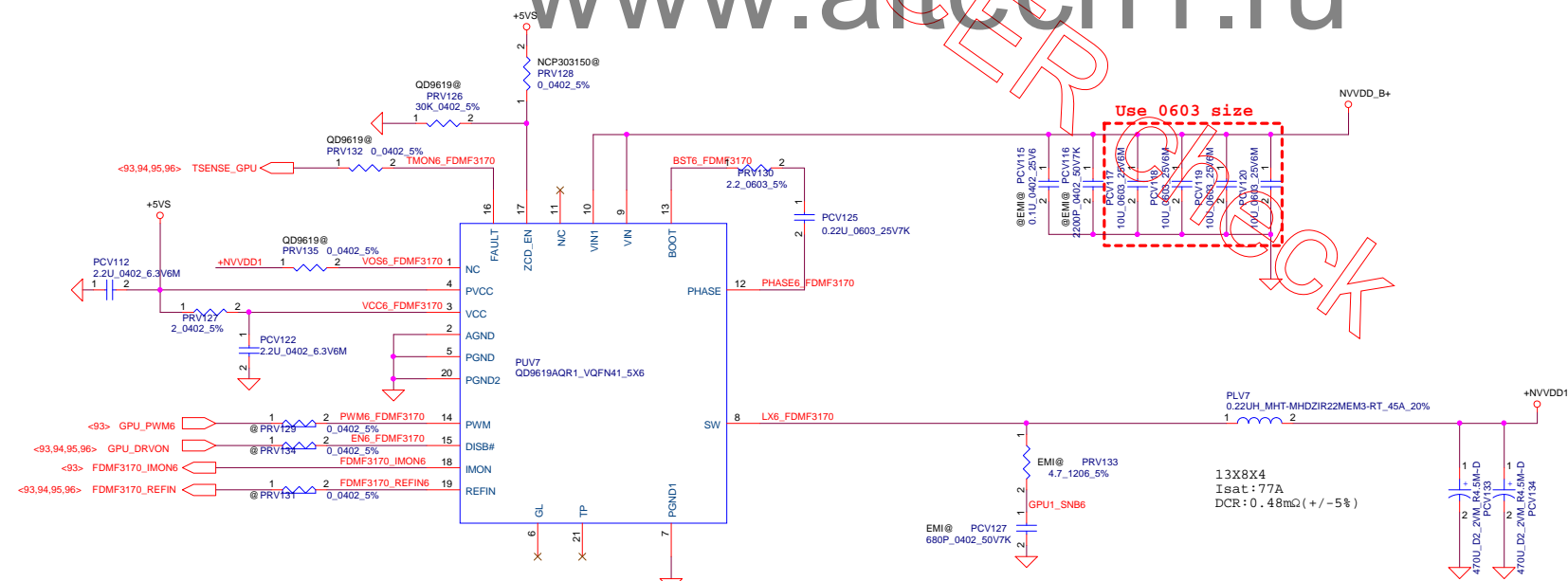
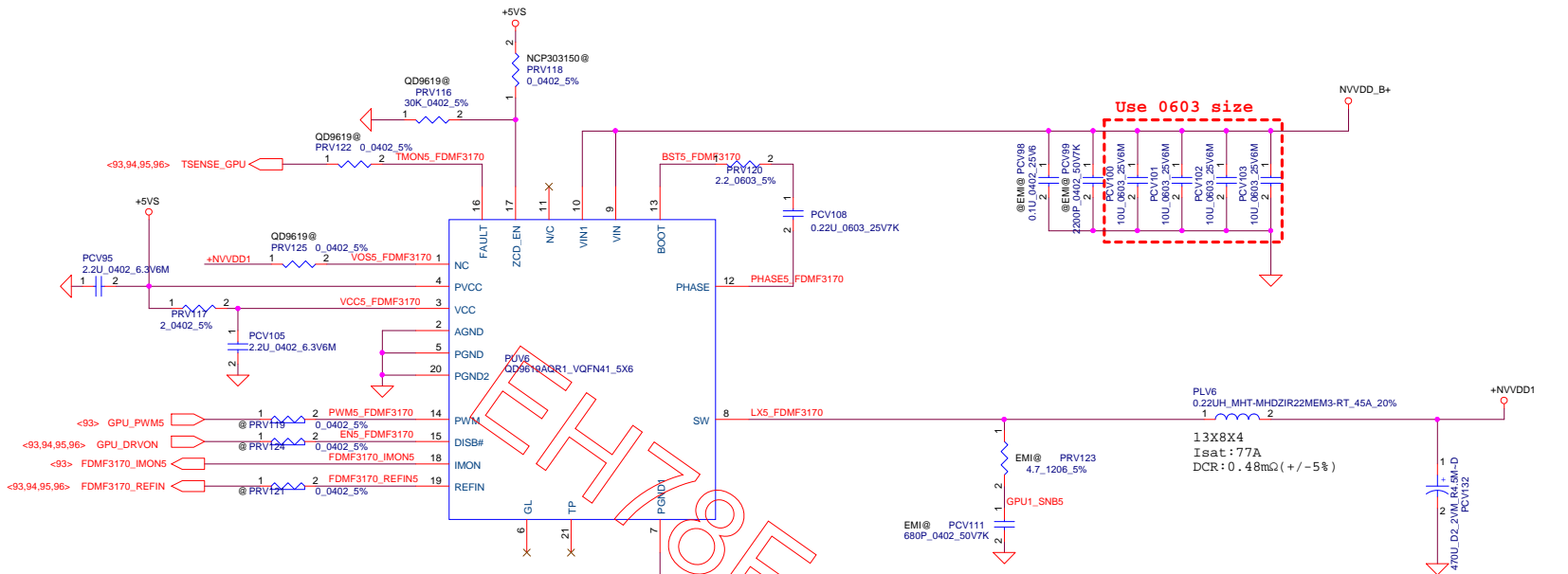


NVVDD1  
TDC 156A  
Peak Current 460A  
OCP 552A  
DCR=0.48 mohm +/-5%

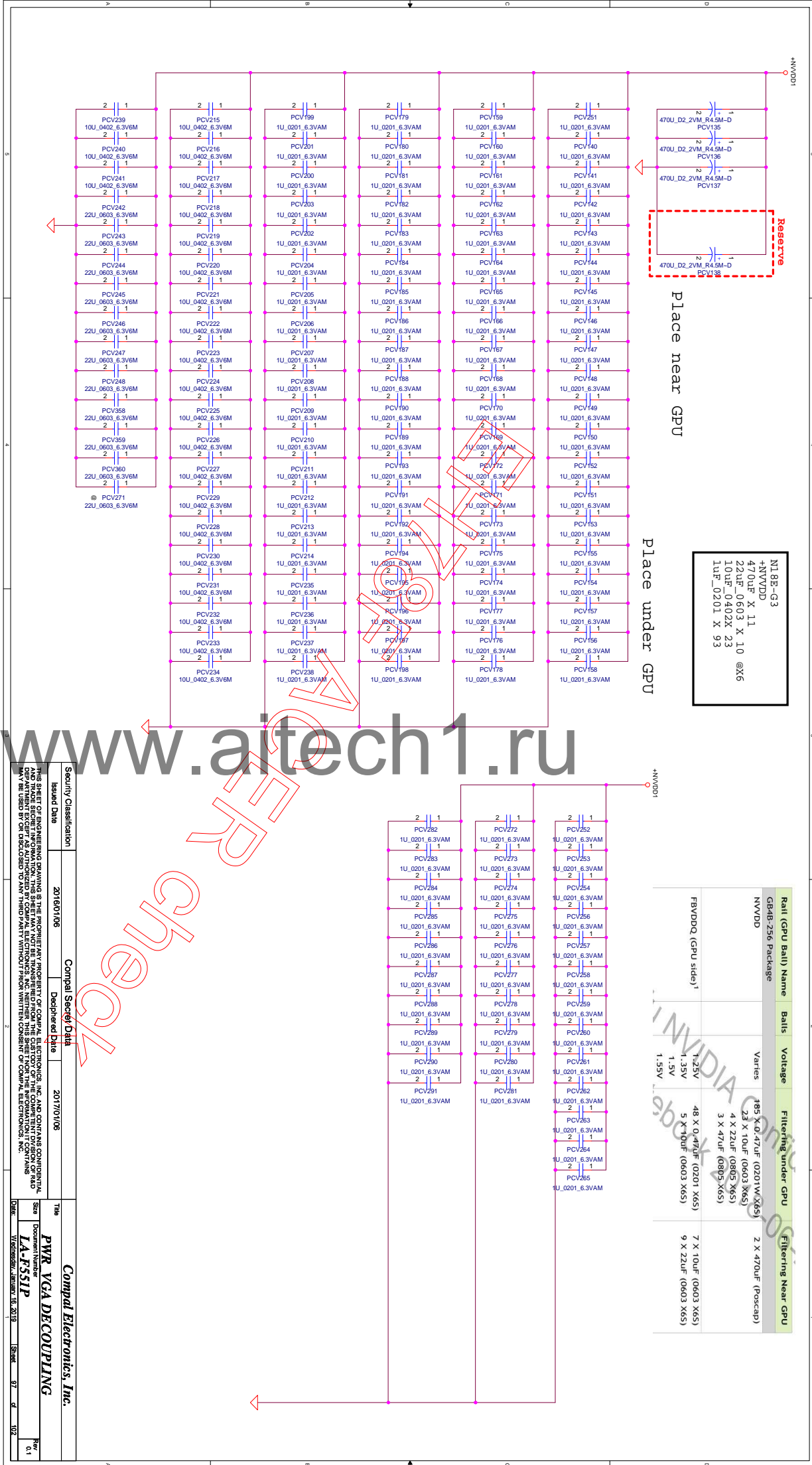
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LA-F551P		Date		Wednesday, January 16, 2019	
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Size	Document Number	Rev		0.1	
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Place near GPU

Place under GPU

N18E-G3
+NVDD
470uF X 11
22uF_0603 X 10 @X6
10uF_0402X 23
1uF_0201 X 93

Rail (GPU Rail) Name	Bails	Voltage	Filtering under GPU	Filtering Near GPU
GB48-256 Package				
NVDD		Varies	185 X 0.47uF (0201W X65)	2 X 470uF (Pocap)
			23 X 10uF (0603 X65)	
			4 X 22uF (0805 X65)	
			3 X 47uF (0805 X65)	
FVDDQ (GPU side)¹			48 X 0.47uF (0201 X65)	7 X 10uF (0603 X65)
			1.25V	9 X 22uF (0603 X65)
			1.35V	
			1.5V	
			1.55V	

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Declassified Date		
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Size	Document Number	Rev
1A-F531P		1.1
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PWR VGA DECOUPLING



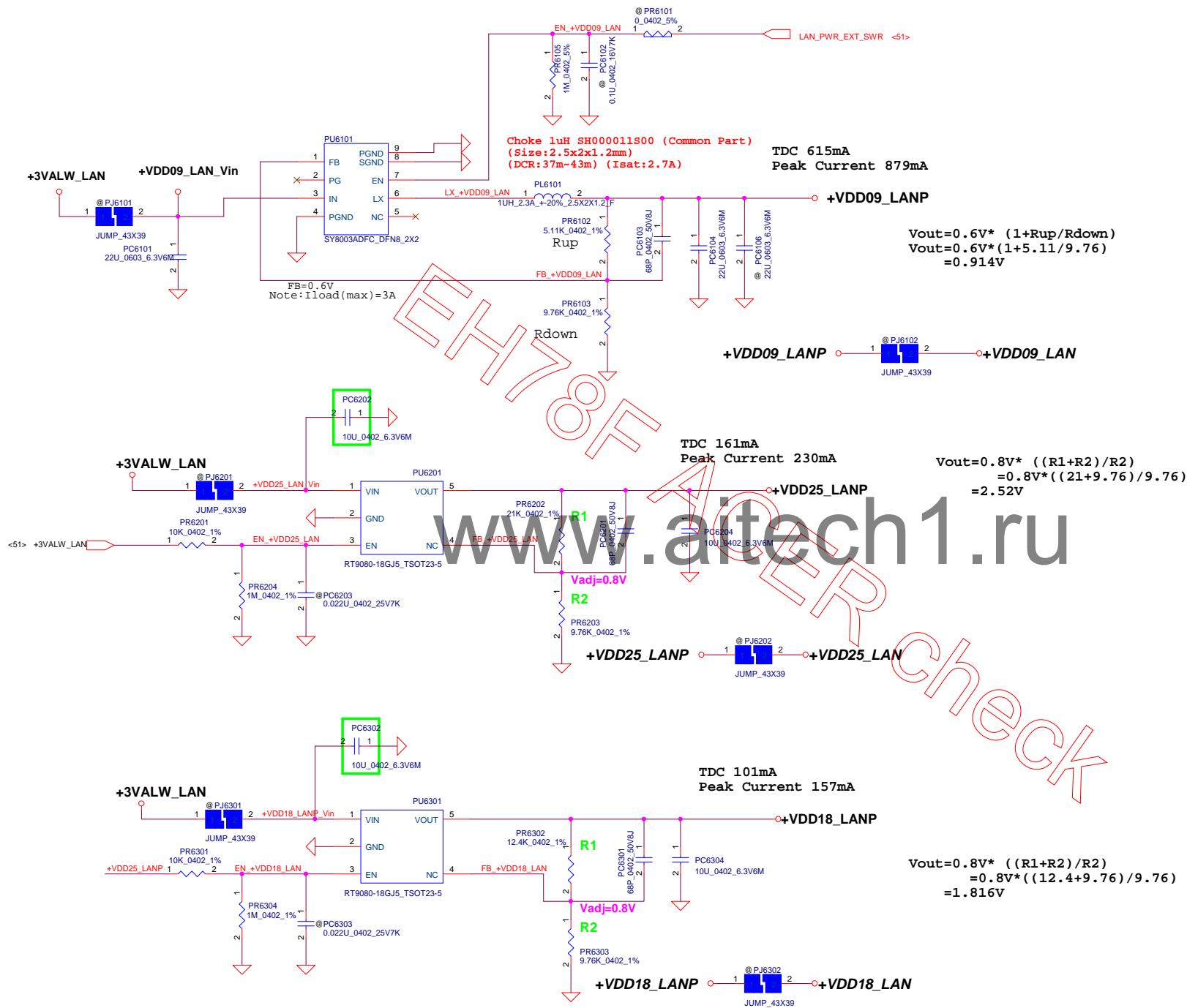


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Title			<Title>
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Item	Page	Title	Date	Request Owner	Solution Description	Rev.
1	P82	design change	10/8		pu201 G718_SA00003K300 change to unpop	0B
2	P86	design change	10/8		PD1501 change from SS1P4_SCS00006P00 to SS3P4_SCS00005H00 Add PR1512 0ohm_SD028000080	
3	P83		10/8		PQ307 & PQ308 change footprint	
4	P85		10/8		Add PD501_SCS00009P00	
5	P101		10/8		PR6102 change from 1.33k_SD00000RF00 to 5.11k_SD034511180	
6	P93		10/8		PRV139 & PRV140 change from unpop to SMT 10k_SD034100280	
7	P98		10/8		PR1017 change from R_short to 0_SD028000080 PQ1003 change from 2n7002_SB00000ST00 to DMN53_2N_SB00001DD00	
8	P101		10/12		PU6301 & PU6201 change from RT9041E_SA00006K300 to RT9080N_SA0000C0600, because x1 code.	
9	P83		10/12		PQ302 change from L2N7002_SB00000ST00 to 2N7002_SB000009Q80 for 2nd source	
10	P98		10/15		Add PC1035 PC1036 220u_D7_SGA0000AM00	
11	P100		10/15		PR1608 change from 15k_SD034150280 to 21.5k_SD034215280	
12	P89	design change	10/17		PC825 change from 100p_0402_SE071101J80 to 470p_0402_SE071471J80 PR841,PR845,PR846,PR849 change from 115k_0603_SD014115380 to 130k_0603_SD014130380 PR811 change from 1.78k_0402_SD00000WY80 to 1.65k_0402_SD034165180 PR813 change from 31.6k_0402_SD034316280 to 29.4k_0402_SD034294280	
13	P92		10/17		PC9025,PC9026,PC9050 220u_D7_SGA0000AM00 change to unpop	0C
14	P98		10/19		1.35Vsdgpu add PC1037 560u_D2_SGA00006J00 PC1030, PC1031 change from 560u_D2_SGA00006J00 to 220u_D7_SGA0000AM00 add PC1038, PC1039, PC1040 220u_D7_SGA0000AM00	
15	P97		10/19		add 1u_0201_PC272~PC291, total 20pcs.	
16	P83		10/22		PR328 change from 200k_SD034200380 to 21.5k_SD034215280	
17	P97		10/22		remove @ 22u_0603_SE00000M000, PCV266,PCV267,PCV268,PCV269,PCV270	
18	P98		10/22		PR1004 change from 383k_0402_SD034383380 to 442k_0402_SD034442300	
19	P98		10/25		PR1010 change form 4.64k_SD00000K980 to 4.02k_SD034402180 PC1008 & PC1037 change form 560u_D2_SGA00006J00 to 330u_D1_SGA00009S00	
20	P84	HW request	11/5		PR402 change from 6.65k_0402_SD034665180 to 7.15k_0402_SD034715180	
21	P99	HW request	11/27		PC1106 change to unpop, for sequence	
22	P93		11/30		add PRV155 0ohm_0402 PCV9 PUV8 change to un-pop	
23	P83	EMI request	11/30		add PC326 0.1u_0402, PC303, PC305 change to SMT PR102, PC101, PR103, PC104 change to SMT	
24	P83		12/03		PQ308,PQ502 change from aon7506_SB000010A00 to EMB12N03_SB00001HV00	
25		design change	12/03		update PQ306,PQ307,PQ308,PQ401,PQ402,PQ403,PQ404,PQ501,PQ502 footprint to Q_N_DFN33-8-5	
26		design change	12/03		PR312,PR316,PR344,PR329,PR1512,PR801,PR810,PR821,PR822,PR925,PR929,PR927,PR931, PRV20,PRV34,PRV50,PRV155,PRV70,PRV54,PRV56,PRV58,PRV60,PRV62,PRV65,PRV145, PRV146,PRV147,PRV148,PRV149,PRV150,PRV1,PRV12,PRV13,PRV18,PRV79,PRV84,PRV81, PRV89,PRV94,PRV91,PRV99,PRV104,PRV101,PRV109,PRV114,PRV111,PRV119,PRV124,PRV121, PRV129,PRV134,PRV131,PR1016,PR1017,Pr1606,PR1602,PR1603,PR6101 change to 0402_R-short	
27		design change	12/03		PR409,PR410,PR502,PR603,Pr7201,PR1109,Pr1601,PR1604 change to 0603_R-short	
28	P98	design change	12/03		PC1022,PC1045 change from 4700p_SE074472K80 to 2200p_SE074222K80	
29	P86	design change	12/04		PD1501 change from SS3P4_SCS00005H00 to SS32FL_SCS0000FD00	